Chapter 5 : Electronics

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Electronics Introduction

The main purpose of the ANTARES electronics is to provide a hardware implementation in which the following functions can be performed:

- data acquisition/slow control,
- power distribution,
- clock distribution,
- trigger distribution

Technical aspects (mechanics, connections, thermal cooling) concerning all the boards are described in the section on Hardware implementation. The reliability of the offshore electronics is an important issue and requires careful choice of components and testing of the electronics prior to deployment.

The electronics are located in various pressure resistant containers of the detector architecture as summarised in the line structure page or PBS**.** Six main objects are relevant, for the electronics discussion:

- The Local Control Modules (**LCM**) **PBS2.1** contain the electronics for the readout of three Optical Modules (OM) and the various instruments located on a storey. They also contain the electronics of the offshore trigger logic and the local power supply. One LCM, called Master Local Control Module (**MLCM**), is present in every sector and multiplexes in addtion, the signal information from five storeys onto one optical fibre at a wavelength unique to that Storey.
- The String Power Module (**SPM**) **PBS2.3** contains the power supply for the string.
- The String Control Module (**SCM**) **PBS2.2** contains the electronics for the readout and control of the SPM and the instruments located at the bottom of the string.
- The Junction Box (**JB**) **PBS2.4** is the central point of the detector; it has connections to all detector strings and to shore. It contains the power supply for the whole detector and the electronics for conversion of the trigger signals into a global readout request signal. It also distributes the clock signals to all LCMs.
- The electronics for the generation of the master **clock (PBS2.5)** is located at the shore station. The main power supply is also located onshore, in the power hut.

Each detector string consists of 1 SPM, 1 SCM and 30 LCMs. The LCMs inside a string are organised in 6 sectors; each sector consists of 5 LCMs. Each sector has a master LCM which combines the functionality of a LCM with that of network node in the offshore DAQ system.

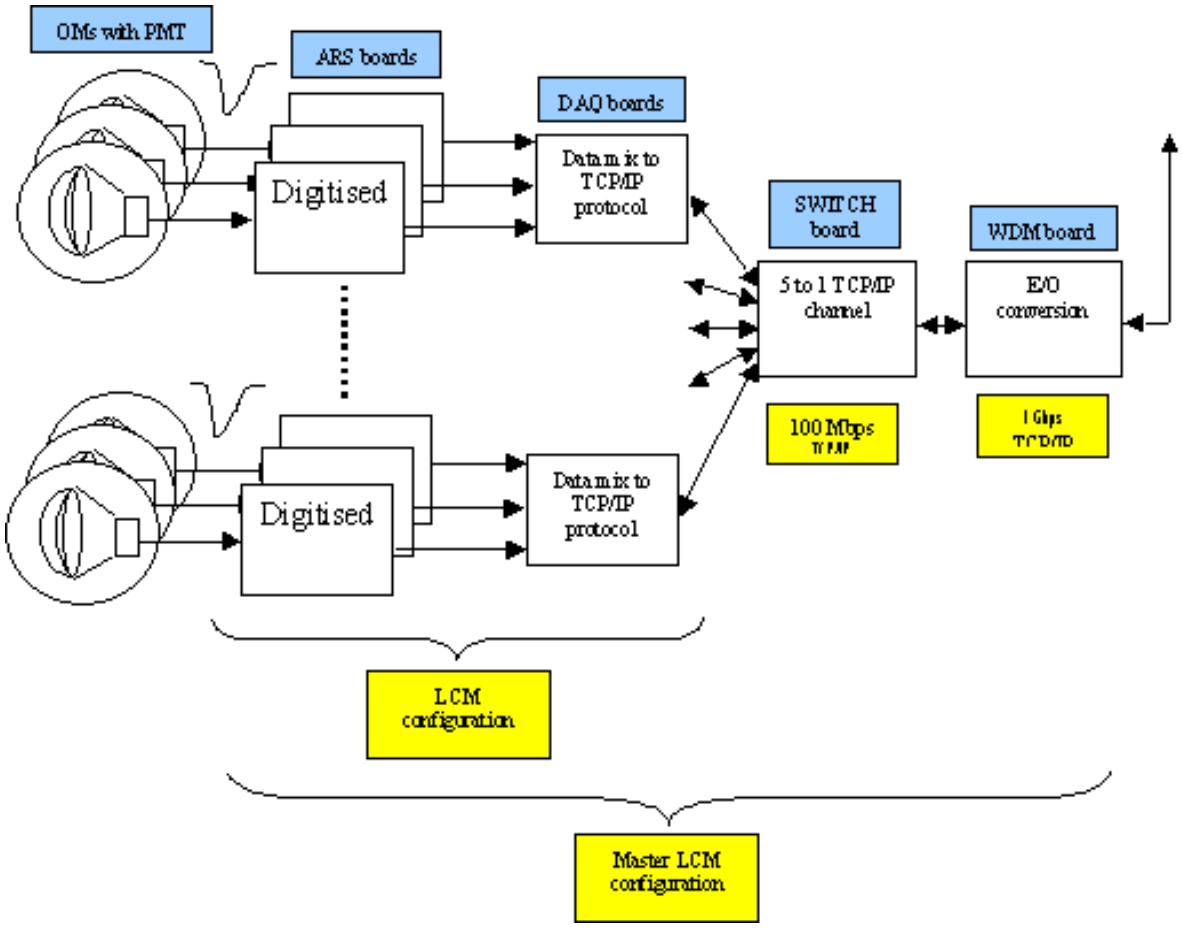
Within each of these containers, a number of electronics cards provide the desired functionality, which are described in the individual object PBS pages. The electronics cards are inserted in a crate and the power and signals are passed between boards via the backplane or via twisted pair wires.

The connection between the various containers are provided by electro-optical cables, the power being transmitted via electrical wires and the signals via optical fibres.

The most relevant technical notes are listed at the end of each section.

DAQ and Slow-control functions

The data acquisition and slow-control functions are described in chapter 4. The electronics implementation is described here. The readout chain is summarised in the figure below.



Functional schematic of the DAQ electronics

The analog output signal of each PMT is processed by two Analogue Ring Sampler (ARS) chips located on the ARS motherboard (ARS_MB). The ARS produces a time-stamped digitisation of the PMT signal. Two digitisation modes are possible: Single Photo Electron (SPE) and WaveForm (WF). A SPE event contains only the total charge of the PMT signal, whereas the WF contains also a waveform sampling of the PMT output.

When a L1 or L2 trigger (for a definition, cf Chapter 4 on offshore trigger) is received, the ARS begins the digitisation of the analog signal inside the analog pipeline for WF sampling or internal charge integration for the SPE event; the resulting digital data packet is sent over the chip serial output to the DAQ board. If no trigger is received within a fixed latency, the signal is discarded.

The bandwidth of the readout system is increased using a Dense Wavelength Division Multiplexing (DWDM) and Ethernet switches. Its implementation is summarised in Figure 2.

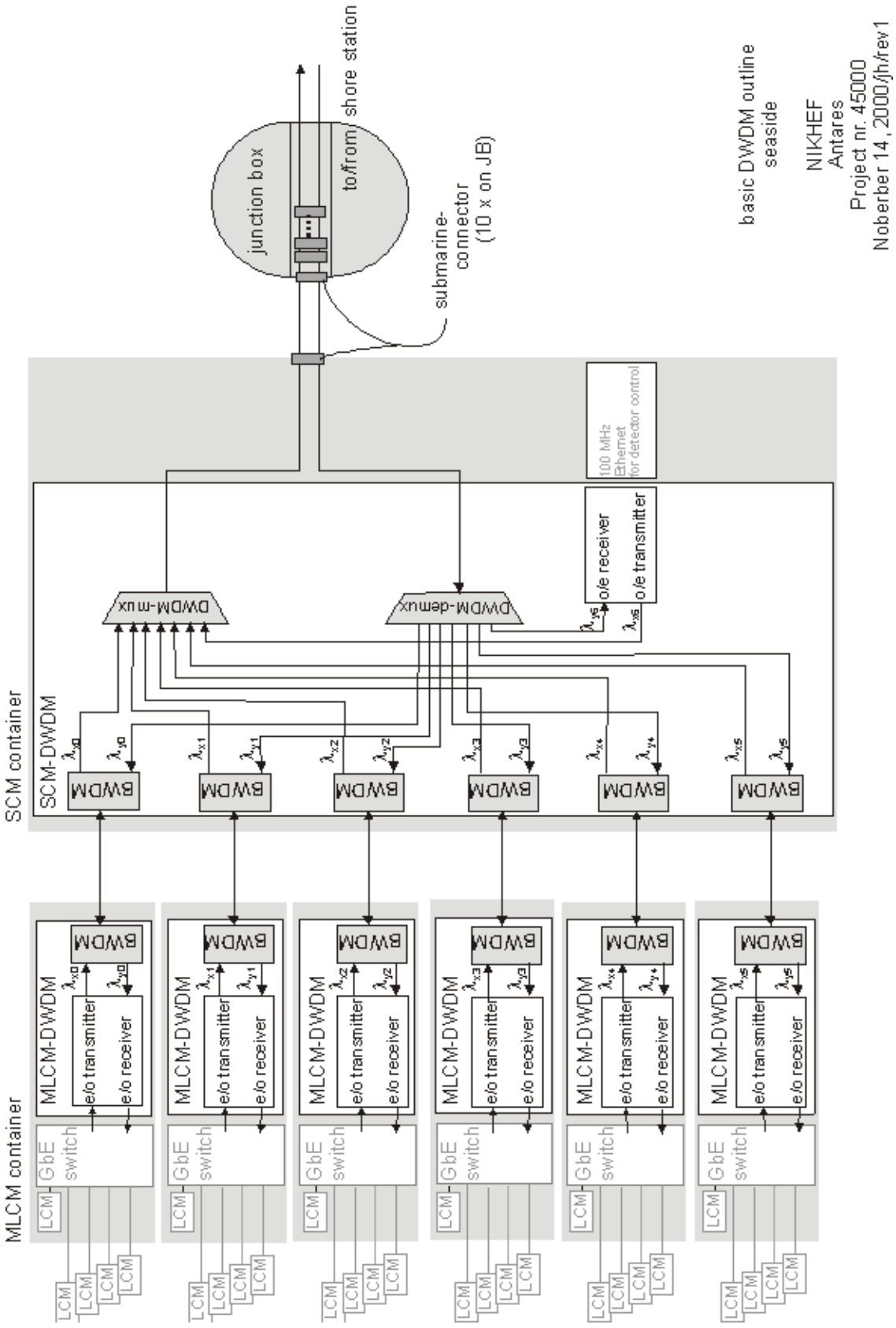


Figure 2: The offshore DWDM system

At the DAQ board of an LCM (LCM_DAQ/SC) the data produced by three ARS motherboards is transmitted using the BIDIANT transceiver board, via optical fibre (1310 nm) to the MLCM. At the MLCM, the data from the five LCMs (MLCM + four slaves) are received by a bi-directional Ethernet concentrator board (LCM_BIDICON) and the optical signals are converted to electrical

signals. The signals are passed via the backplane to the MLCM_SWITCH board where the five sets of signals are combined and then passed via coaxial SMB connectors to the MLCM_DWDM board. This board converts the gigabit Ethernet signals into optical signals of a DWDM system (1535 nm-1570 nm) and sends them to the SCM.

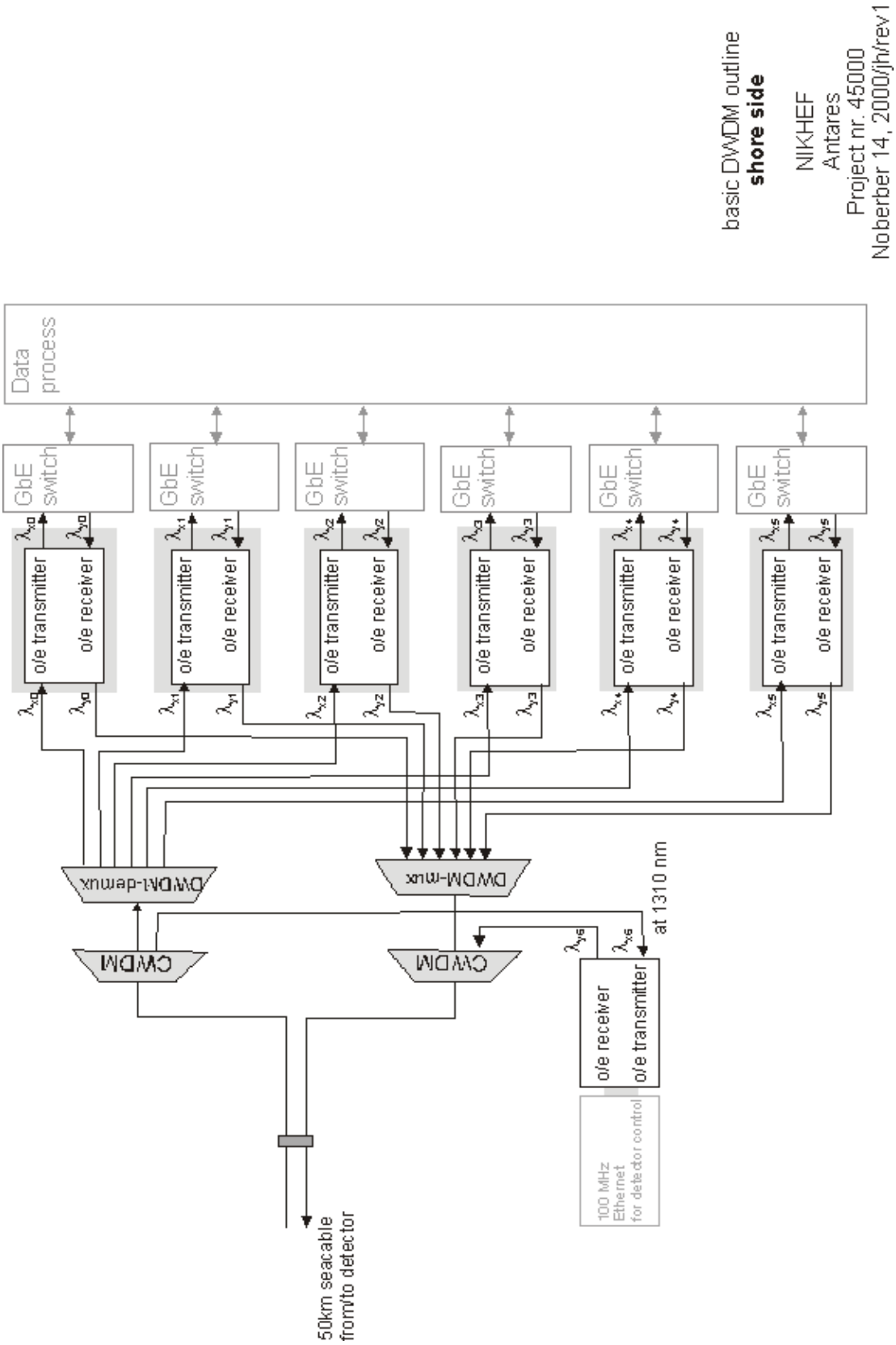


Figure 3: The onshore DWDM system

At the SCM, the optical signals from the six MLCMs of a string, are received by a passive optical multiplexer (SCM_DWDM_MUX) and combined onto a single fibre, each MLCM having its unique pair of wavelengths. The Slow Control information is also included in the wavelength multiplexing as a seventh wavelength. In order to do this, the Slow Control information passes through the SCM_DWDM board prior to inclusion. The data then passes through the Junction Box to the shore station. An equivalent system on shore, demultiplexes the wavelengths as shown in figure 3.

The optical power budget, including all connections and feed-throughs in the optical path, has been studied for the DAQ, clock and trigger distribution (see Technical Note 3 LCM 13 01 A). The worst case is that of the DAQ distribution for a signal traversing the whole length of a string. This situation is summarised in the following table.

Optical losses of the DAQ distribution

MLCM-DWDM (top) to DWDM-mux 30 OPTOCLIP connectors	-3.0 dB max
57 penetrators: 0.01dB/penetrator	-0.6 dB
EMC: 350 m SMF28	-0.1 dB
DWDM-MUX	-3.6dB max
splice DWDM to fibre	-0.2 dB
splice in SCM	-0.1 dB
wetmateable jumper connector	-0.75 dB
interlink cable from SCM to JB: 500m	-0.1 dB
wetmateable jumper connector	-0.75 dB
internal JB splice	-0.1 dB
JB connector to MEOC	-1.5 dB
MEOC: 50km ALCATEL cable	-10.0 dB
Splice MEOC to shore fibre	-0.1 dB
shore fibre: 5 km SMF28	-1.0 dB
splice shore fibre to broadband monitor splitter 1%	-0.2 dB
splice broadband monitor splitter to DWDM	-0.2 dB
DWDM Demux	-3.6dB max
splice DWDM-Demux to Detector	-0.2 dB
Avalanche Photo Diode	-0.3 dB
Total optical loss of passive network	~ -26 dB

Assuming a laser output power of 6 dBm and an avalanche phtodiode receiver with a (typical) sensitivity of -30 dBm, this implies a power margin of 10 dB. This margin is sufficient to compensate for normal ageing effects during the lifetime of the experiment. In order to reduce optical losses and increase reliability, fusion splicing of the optical fibres will be used wherever possible.

The electronics implementation of the Slow Control is ensured by the UNIV daughter board. The UNIV board is based on a RS485 driver chip and uses the MODBUS protocol. It is described in

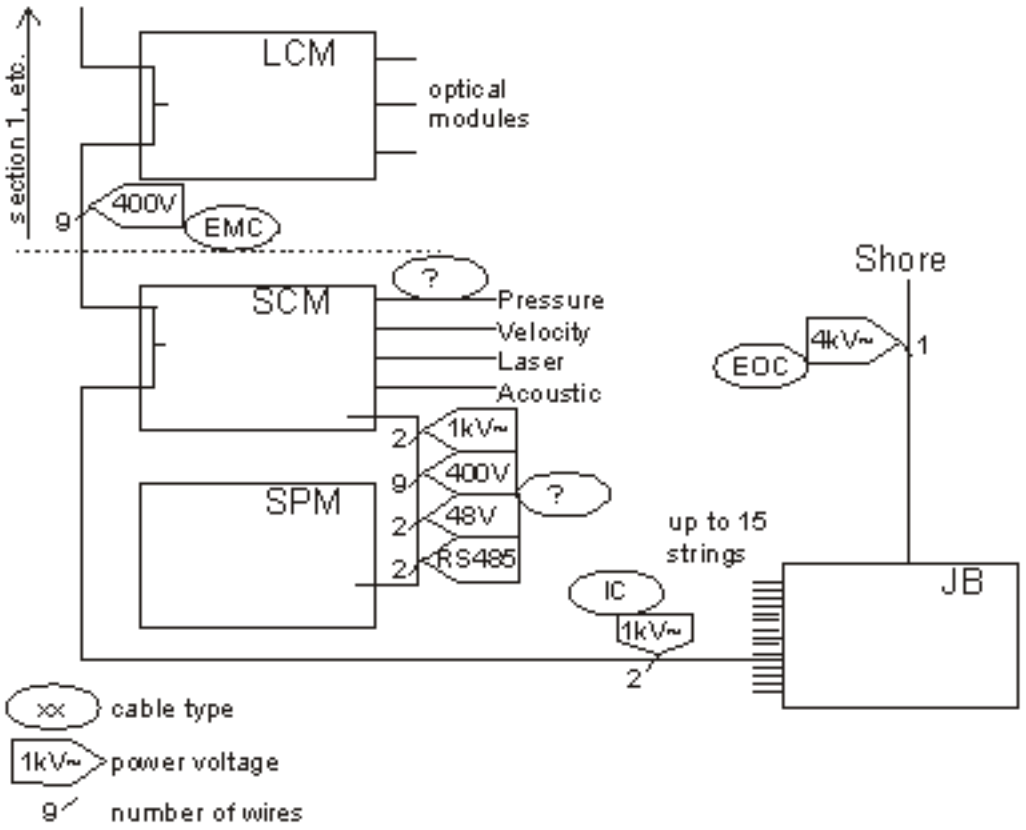
detail in the technical notes 3 LCM 08 01/A and 3 LCM 08 02/A. The instruments which have a RS232 link require a dedicated bridge.

Technical notes are available for more details:

- 3 LCM 15 01A: ARS motherboard description.
- 3 LCM 05 01 A: LCM_DAQ/SC board description
- 3 LCM 13 01 A: Design specifications for the ANTARES DAQ- DWDM Network- Part I
- 3 LCM 13 02 A: Design specifications for the ANTARES DAQ- DWDM Network- Part II
- 3 LCM 20 01 A: LCM internal organisation
- ANTARES-Elec/2000-6: ARS1 Analogue Ring Sampler & ARS_CONV Users Manual Version 1.9
- 3 LCM 08 01/A UNIV1 board user's manual
- 3 LCM 08 02/A. MODBUS protocol reference guide.

Power distribution

The distribution of power from the shore up to the level of the SPM is described in the Power section in chapter 7. In this section, its implementation inside the SPM and the LCM are discussed. A summary of the power distribution is displayed in the figure below.



Schematic view of the Power distribution

The Junction Box provides each String Power Module (SPM) with 1000 Vac. The SPM converts this voltage value to 400 Vdc which feeds the DC-DC converters of the POWER_BOX within the LCM. The SPM also provides 48Vdc for use in the SCM and internally for the Slow Control functions of the SPM.

Power consumption of all the boards in the different LCM configurations was estimated: each MLCM needs a total of 31.94 W, each LCM slave 1 needs 23.9 W, LCM slave 2, 20.84 W and LCM slave 3 18.9 W. Details are given in technical note 3 LCM 20 05/A.

Clock Distribution

The main purpose of the clock system is to provide a common clock signal to all ARSs. It consists of a clock generator on shore, a clock distribution system and a clock signal transceiver in each LCM. In addition, it can distribute a (small) number of other commands to the LCMs. These commands can be addressed to a single LCM or to all LCMs simultaneously. The same clock is also used by the acoustics positioning system.

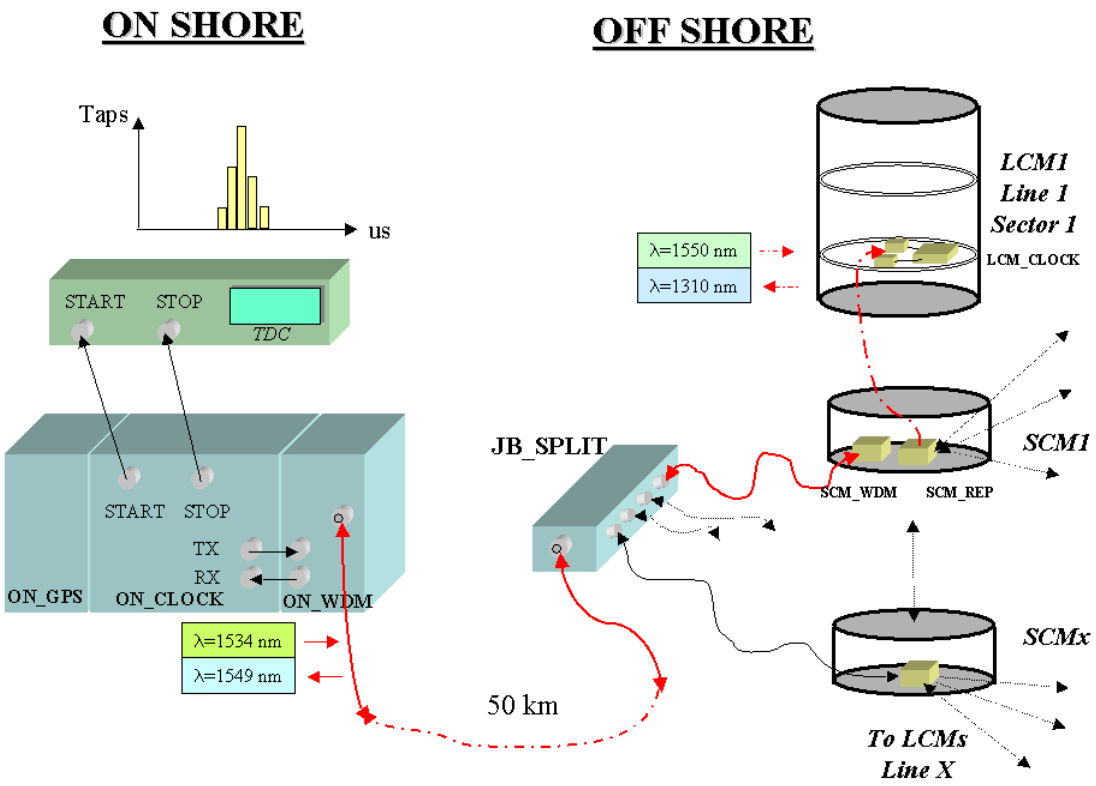
The main specifications of the clock system are:

- generation of a 20 MHz clock signal
- Distribution of the (common) clock signal to all LCMs
- Distribution of (synchronised) data commands for common orders like DAQ *start* or *stop* run.
- Time stability better than 0.5 ns
- Time correlation with the GPS time better than 100 ns.
- Possibility to measure delay propagation between on shore to each LCM or SCM container with a precision better than 1 ns, for time calibration.

The clock system is based on the network synchronisation concept used in the telecommunications industry in which digital data are superimposed on a high frequency reference clock. The combined signal is sent to the detector and distributed to all LCMs. In each LCM the original clock signal and the data are decoded.

A functional diagram of the clock system is shown below. The reference clock is generated on shore (ON_GPS) using a high accuracy 20 MHz clock synchronised internally to the GPS time with an accuracy of 100 ns. The clock is passed to the ON_CLOCK board where any clock commands are superimposed. The clock electrical signal is converted to an optical signal in the ON_WDM board which transmits the signal to the Junction Box, via a single optical fibre, using standard telecommunication transceiver chips (HOTLINK chips from Cypress company). With this configuration, the time jitter was measured to be less than 100 ps.

A passive splitter inside the Junction Box (JB_SPLIT1) divides the optical clock signal into 16 different channels, one for each string (plus spares). Inside the SCM, an Optical/Electrical conversion (SCM_WDM) regenerates the signal and an Electrical/Optical conversion (SCM_REP) sends the clock signal to the LCM_CLOCK board of each LCM container. The LCM_CLOCK board reconstructs the clock and decodes any associated command, making them available on the LCM backplane.



Clock distribution

The actual implementation of the clock distribution network is based on a bi-directional communication system. Between the shore and the JB, the 1534 nm and 1549 nm wavelengths are used. In the detector (ICC and EMC), the 1310 nm and 1550 nm wavelengths are used.

The return path is used to measure the propagation delay between the on-shore clock system and the LCMs in the detector. This delay is measured using a commercial Time to Digital Converter (SRS620, Stanford Research company). A precision of better than 0.5 ns on the propagation time from shore to the addressed LCM (only one LCM is addressed at a time) has been obtained. The return signal capability is also used to send data (DAQ-CLK-STATUS) to shore for test and debugging.

The complete list of data commands that can be transmitted by the clock system are given below:

CLK-ARS-RST-TS reset time stamp of all ARSs (global)

CLK-ARSi-LED-PL generation of a LED pulse

CLK-ARS-ENA enable/disable the ARS (addressable)

CLK-DAQ-RST hardware reboot of processor

CLK-DAQ-ENA enable/disable DAQ processors

CLK-TRIG-ENA enable/disable off-shore trigger

CLK-TRIG-PULSE enable temporarily the off shore trigger

CLK-AC-RST1 acoustic reset (slow)

CLK-AC-RST2 acoustic reset (fast)

Details of this clock distribution are described in the technical notes:

- 3 LCM 03 01/C: Numerical clock distribution proposal
- 3 LCM 03 02/A: Clock board interface
- 3 LCM 18 02/A: Clock distribution prototype tests
- 3 LCM 20 01/A: BIDIANT user manual

Trigger system

The offshore trigger is described in detail in chapter 4, the electronics implementation is presented here.

The offshore trigger allows the selection of a subsample of the total data flow for digitisation, transmission and processing on shore. The trigger is based on time coincidences of signals between optical modules of the same storey and also between adjacent storeys.

In order to construct the trigger, the ARS mother board (ARS_MB) produces signals corresponding to whether the output of the each of the three PMTs has passed a lower threshold (L0) or a higher (L00) threshold (the thresholds are programmable via Slow Control). These signals are sent, via the LCM backplane, to the LCM trigger board (LCM_TRIG). Here a decision, based on time coincidences between the six set of signals, is made as to whether to read out just the local triplet of OMs (a L1 trigger) or to initiate a global readout request (L2 trigger).

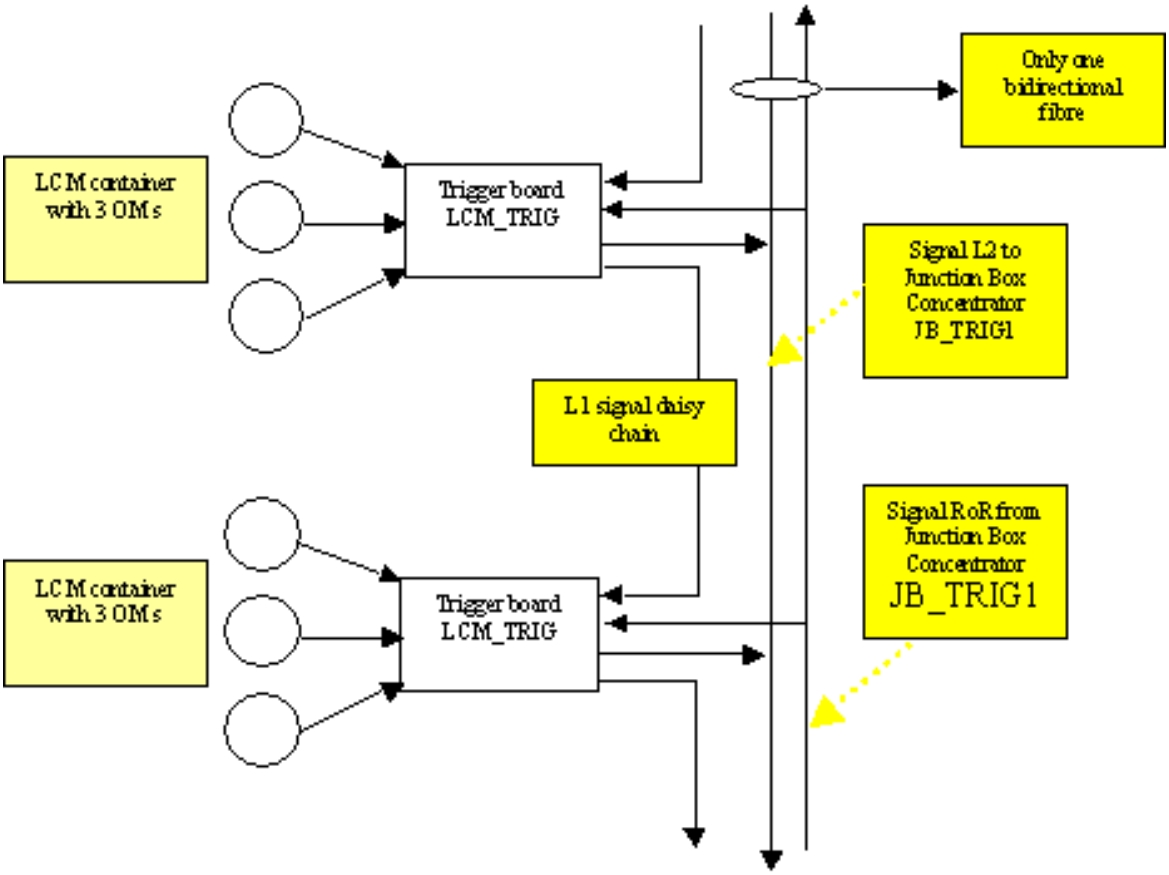
If a L2 trigger is generated it is passed, via the SCM, to the Junction Box trigger board (JB_TRIG1). Here, the L2 triggers from all lines are optically merged (ORed) using a passive optical splitter. The output of the splitter is regenerated (using a BIDITRIG board) and retransmitted at a different wavelength, through the same optical splitter back to all the LCMs as the Read Out Request (RoR).

The trigger construction in the LCM trigger board (LCM_TRIG) is performed using a Field Programmable Gate Array (FPGA). A local oscillator (100 MHz) is used to generate the delays and pulse widths for the various trigger signals with a precision of 10 ns. All the necessary trigger requirements, delays and pulse widths are definable by Slow Control using the UNIV1 board.

The L1 signal from an upper storey is passed via a single optical fibre to a lower storey, where it can also be used in the construction of the L2 trigger decision of that storey.

The L2 and RoR signals are bi-directional on one optical fibre of the EMC. The L2/RoR optical fibre is daisy chained the whole length of a string. As the signals propagate down (L2) or up (RoR) the EMC cable, they pass through many other LCM_TRIG boards and are regenerated each time in a BIDITRIG daughter board.

Two optical fibres (plus two spares) in the Main Electro-Optical Cable (MEOC), are used to test and monitor the offshore trigger. They are connected to the JB_TRIG board of the JB.


Only one bidirectional fibre
LCM container with 3 OMs
Trigger board LCM_TRIG
Signal L2 to Junction Box Concentrator JB_TRIG1
L1 signal daisy chain
Signal RoR from Junction Box Concentrator JB_TRIG1
LCM container with 3 OMs
Trigger board LCM_TRIG

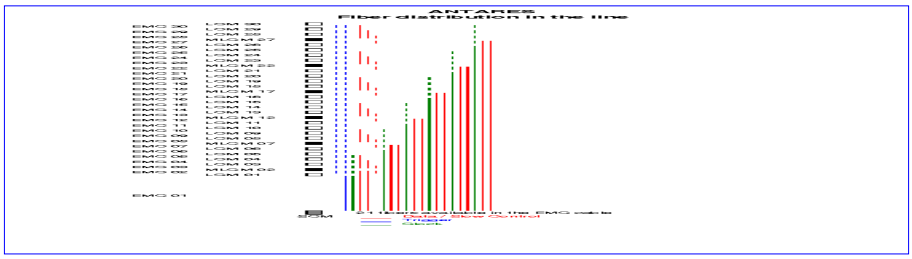
Schematic view of the offshore trigger.

Hardware implementation

The Electro-Mechanical Cable

The connections between the SCM and the LCM are made by the electro-mechanical cable (EMC). It comprises 9 copper wires for power distribution and 21 optical fibres for data transmission.

For the DAQ, each MLCM is connected to the SCM by one pair of optical fibres. Each LCM in a sector is connected to its MLCM by a single (bidirectional) fibre. For the distribution of the clock signal, the bottom LCM of a sector is connected to the SCM by a single fibre; the same fibre is used to daisy-chain the signal through the sector. The L2 trigger and readout request signals are daisy-chained through the entire string on a single (bidirectional) fibre. One additional fibre is used to transmit the L1 trigger between storeys. The total number of fibres is thus 2*6 +1(daq+sc) + 6 (clock) + 2 (trigger) = 21. A schematic of the fibre connections is shown below and can be seen better by clicking here on on the icon:



The electrical power distribution in the EMC has a similar organisation. The bottom LCM of each sector is connected to the SPM by a single copper wire. The same wire is used to daisy-chain the power distribution to the other LCMs of the same sector. The return current of two sectors is combined into one copper wire. Thus, a total of 9 wires is is needed for the electrical power distribution on the string.

The connection between the SPM and the SCM passes through a sleeve joining the two modules. This allows the power in the SPM to be separated from the optical fibres in the SCM.

The Interconnecting Link

Each detector string is connect to the JB by an Interconnecting Link (IL); the interconnecting cable of the IL has 2 copper wires and 4 optical fibres. The copper wires are used to transfer power from the JB to the SPM. The optical fibres transmit signals between the JB and the SCM; two fibres are used for the DAQ, one for the clock, and one fibre transmits both the L2 trigger and the readout request.

The Main Electro Optical Cable

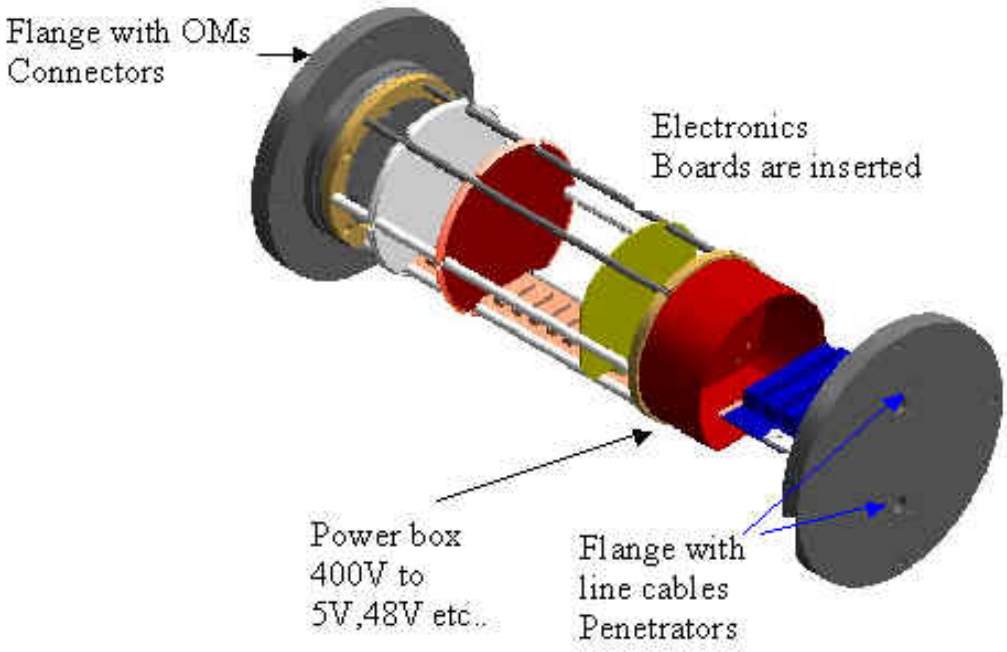
The JB is connected to shore by the Main Electro-Optical Cable (MEOC). The MEOC has 48 fibres and one copper sheath. The sheath is used to distribute the power from the power hut; the return current flows through the sea water. For the DAQ, the JB connects each pair of optical fibres of a string to a corresponding pair of optical fibres in the MEOC. A single optical fibre (plus a spare) is used for the distribution of the clock signal. In addition, 2 optical fibres (plus 2 spares) are

used to test and monitor the off-shore trigger system. The number of fibres in the MEOC is sufficient to allow for a larger number of detector strings than presently foreseen.

Containers

The electronics boards are mounted in pressure-resistant titanium containers. A mechanical description of the containers is given in chapter 2 on mechanics. Inside these containers, the electronics boards are mounted on a common backplane. The boards are mounted perpendicular to the backplane and can be exchanged independently. All boards have the same dimensions. The following figure shows the crate with the power supply and some boards.

Electronics crate prototype with inserted boards and the POWER_BOX



The thermal cooling of the electronics is ensured using copper screens inserted between the electronics boards. These screens are in contact with the titanium container, maintained at the ambient sea water temperature (14°) via flexible copper 'fingers'. Hot electronics components are connected directly to these screens via a thermal bridge. Laboratory measurements show that a thermal resistance of 17°/watt can be obtained using this method (see internal note 3 LCM 18-04/A).

The copper screens have a secondary function of providing electromagnetic shielding between sensitive analog functions such as the ARS motherboard (ARS_MB) and noisy digital functions such as the MLCM_SWITCH.

For the electrical connections, soldering is adopted in order to minimise the risk of oxidation of connector contacts. All connectors between the boards and the backplane are gold-plated.

For the optical connections, fusion splicing is adopted wherever possible. When necessary, optical connectors will be used (OPTOCLIP II). After qualification tests, connectors from the Deutsch company have been chosen; they have the following features:

- Optical power loss: average 0.07 dB per connector (max 0.1 dB). For the worst case of a signal traversing the 30 connectors of a complete line, the

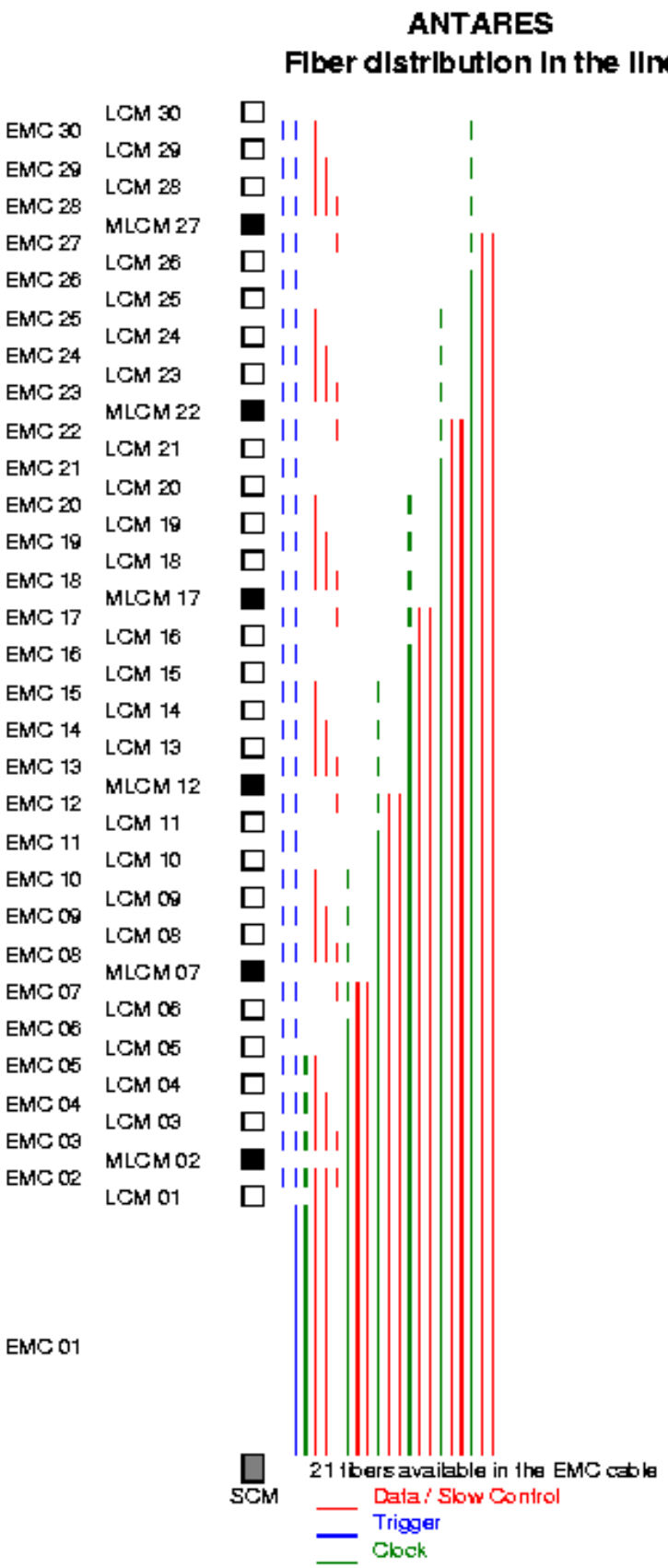
maximum optical power loss is 3 dB.

- Reliability of plugging/unplugging: better than 0.05 dB
- Reliability in time: better than 40 years

All the OPTCLIP II connectors are located on the LCM_OPTCON card.

Associated Technical Notes:

- 3 LCM 13 01 A Design Specifications for the ANTARES optical DAQ-DWDM Network, Part I.
- 3 LCM 18 04/A Thermal tests for LCM container
- 3 LCM 20 01/A LCM internal organisation, for the electronics function implementation inside this container.
- 3 SCM 20 01/A SCM internal organisation, for the electronics function implementation inside this container.
- 3 LCM 20 02/A LCM/SCM boards mechanical dimensions and backplane connector implementation.


ANTARES
Fiber distribution in the line
EMC 30
EMC 29
EMC 28
EMC 27
EMC 26
EMC 25
EMC 24
EMC 23
EMC 22
EMC 21
EMC 20
EMC 19
EMC 18
EMC 17
EMC 16
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LCM 16
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LCM 14
LCM 13
MLCM 12
LCM 11
LCM 10
LCM 09
LCM 08
MLCM 07
LCM 06
LCM 05
LCM 04
LCM 03
MLCM 02
LCM 01
SCM
21 fibers available in the EMC cable
Data / Slow Control
Trigger
Clock

Reliability, Qualification and Accelerated Stress Test

The reliability of the offshore electronics is crucial for the long term operation of the detector. The objectives for the overall reliability of the detector are discussed in Chapter 10.

There are three ways to optimise the reliability of the off-shore electronics:

- Choose the components in order to have the best mean time between failure, compatible with availability, price and power requirements
- Require that all designs pass an electronics qualification test before adoption, based on the expected environmental life profile.
- Define a common burning test scenario in order to eliminate bad manufacturing and infant mortality.

Electronics qualification

In order to improve the reliability, the environmental life profiles of the embedded electronics have been studied, resulting in the following qualification tests for the design, which will be verified on the first boards:

- Cold temperature: Storage at 0°C in a wooden crate during transport
- Dry heat: storage at 60°C in a crate during transport, working a few minutes at + 40°C without its packaging.
- Damp heat: storage at 50°C and 93% relative humidity (RH), container open
- Condensation: Damp heat at +40°C and 93% (RH), container open
- Immersion: Working at 3 metres depth, in 25°C seawater for 24 hours.
- Salt fog: Container closed, on quay for one month with 50°C and 1000 W/m².
- Rain: container closed, on quay for one month
- Thermal shocks: From 50°C air to 15°C seawater.
- Sinusoidal vibrations (transport simulation): 5-55 Hz on container without packaging.
- Half-sinusoidal shocks of 15 g acceleration and 50 Hz on container.
- Free fall: height 700 mm on metallic or concrete floor.

Changes in the external appearance of objects can be tolerated as far as they do not impair the functionalities of the object. The first electronics boards must pass these qualification criteria.

The qualification program is described in technical note: 3 LCM 20 04/A.

Accelerated Stress Testing scenario (AST)

The overwhelming majority of electronics failures are latent (hidden) manufacturing defects. Once a robust design has been qualified, testing for reliable field operation can be done much faster and cost-effectively under stress levels that exceed the end-use specifications. An efficient stress screen is to simulate one year of a product's overall fatigue lifetime. This should eliminate 90% of the front-end life cycle `bathtub curve' of `infant mortality' leaving more than 20 years of `normal use' fatigue lifetime in the product.

The following AST scenario is applied to all electronics cards before integration inside any crate container (cf also 3_LCM 20 04/A.):

- Temperature cycling from 10°C to 40°C, 4 cycles during 2 hours
- Vibration with 3 g acceleration during 30 mn with 50 Hz frequency.

Reference technical note :

- 3 LCM 20 04/A. Electronics qualification and AST scenario

Test Benches and test scenarios

In parallel with the electronics development, the development of the associated test benches and test scenarios is necessary. The tests performed during fabrication and integration can be divided into three main types:

- Test scenarios for each board during the prototype phase: every designer provides a test procedure which describes the test set-up and the measurements along with the necessary software and hardware. An example of this test scenario for the clock distribution function can be found in the Web link: 3 LCM 18 02/A Clock Distribution Prototypes Tests.
- Manufacturer acceptation tests: each board realised by the manufacturer or a laboratory must pass a test scenario before acceptation. These tests verify each function of the board and incorporate burning tests (AST scenario). The results of these acceptation tests are directly entered on the Web pages (one per electronics board or object), in order that the results can be incorporated in the general database.
- Main objects integration tests: After the acceptation test of each board, the integration starts with insertion of boards inside the electronics crates. After integration of all these boards, the functionality of the total electronics crate is checked in a test bench, developed to measure and test this complete object. The results of these tests are also entered on the Web pages for incorporation into the general database.

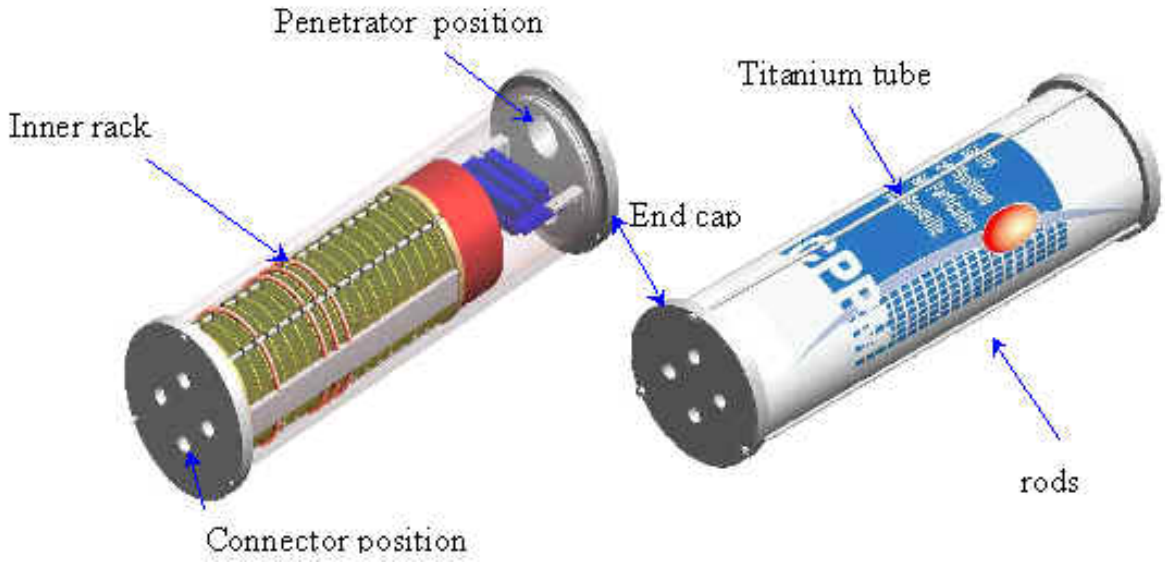
Examples of complete test benches are:

- LCM test bench scenario and for summary web page: LCM test bench schematic
- SCM test bench scenario and for summary web page: SCM test bench schematic

After integration of the electronics boards inside the containers, these final objects are sent for line integration. During the line integration of each LCM container, the good functionality of the electronics and the connections between all objects are tested. These results are also incorporated in the general database.

PBS2.1: The Local Control Module (LCM)

The Local Control Module (LCM) contains the electronics boards for all functionalities at the storey level (readout, DAQ, SC, power, clock and trigger). It is housed in a LCM container, and is linked to the next floors of LCM by 10 m of Electro-Mechanical cable (EMC). The first LCM on the bottom is linked to the SCM/SPM and the last LCM is connected to the Buoy.



In a given sector, there are 5 storeys, one called the 'Master LCM', which has an Ethernet switch, a bidirectional concentrator and a DWDM board that are not in the other LCMs. The 4 'slave' LCMs, are of 3 types:

- slave 1 with acoustic cards,
- slave 2 with LED Beacon
- slave 3 with only the basic boards.

A map of the location of the instruments and LCM types along line 1 can be found here. They will vary from line to line.

Each board inside the LCM is tested in a dedicated test bench. Examples can be found in the technical notes: A test bench of ARS SPE or Preliminary test of clock distribution.

The assembly of the LCM boards and the systematic tests of each LCM is described in the technical note 3 LCM 18 06 A and summarised in Integrated LCM test benches.

List of components inside the LCM

Objects in LCM	Description	PBS number	LCM
LCM Container	Contains the LCM_CRATE with all LCM electronics boards	1.3.002	all
LCM_CRATE	support of boards and backplane	2.1.001	all

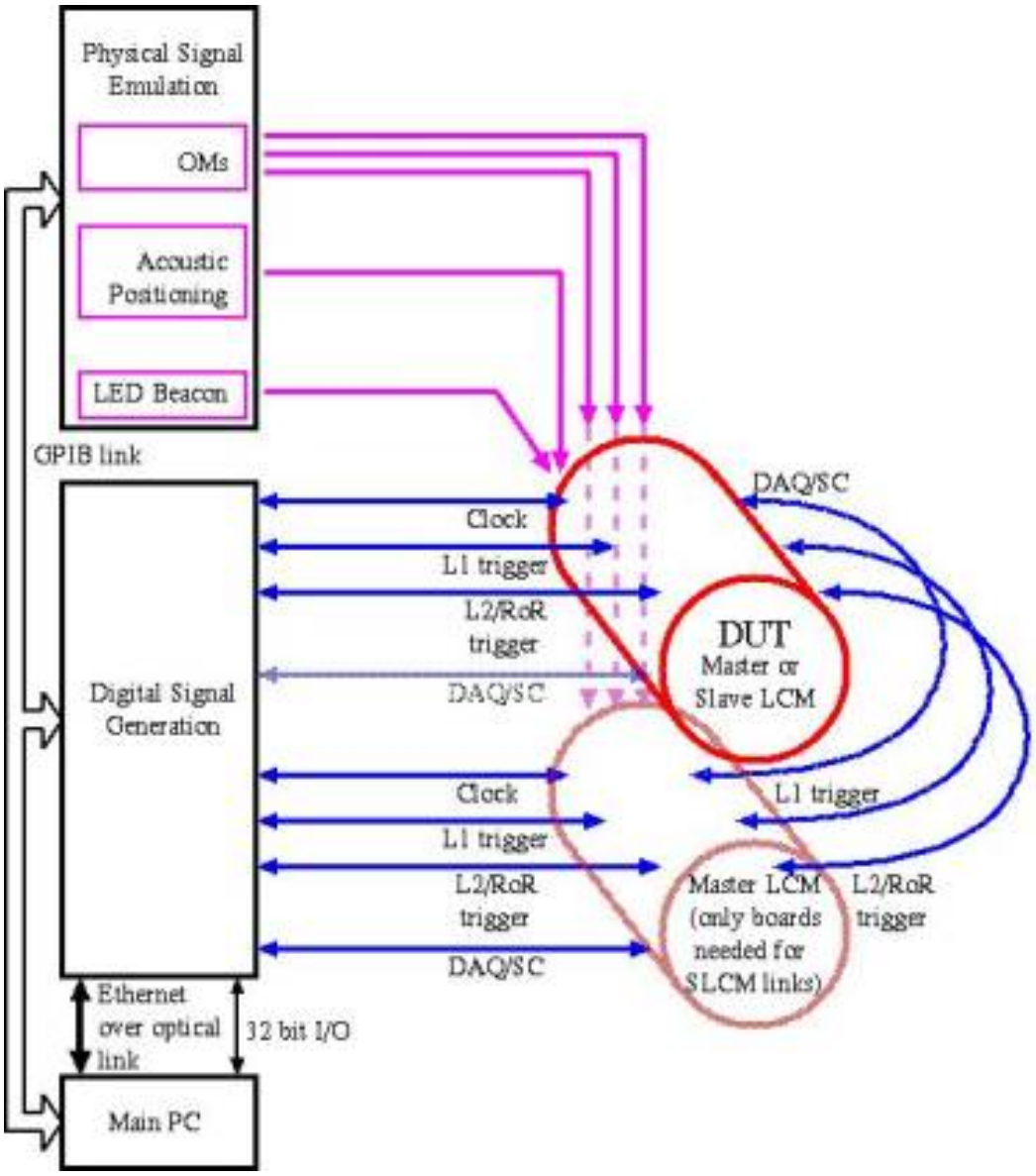
LCM_BACK	distributes signals between boards in LCM_CRATE	2.1.002	all
COMPASS_MB	measures positions with compass and tiltmeters,controls PMT HV	2.1.003	all
ARS_MB	Motherboard with 3 ARS1 chips	2.1.004	all
ARS1	analog pipeline with ADC conversion of PMT signal	2.1.004.1	all
MLCM_BIDICON	Concentrates 4 optical transceivers from each LCM slave DAQ channel	2.1.005	MLCM only
LCM_TRIG	Receives trigger from ARS boards and constructs trigger function	2.1.006	all
LCM_CLOCK	receives optical clock distribution signal and distributes inside LCM crate	2.1.007	all
ACOUST_RX _PREAMP	Positioning system	2.1.008	slave 1 only
ACOUST_RX _DSP	Positioning system	2.1.009	slave1 only
ACOUST_RX _CPU	Positioning system	2.1.010	slave1 only
POWER_BOX	Converts 400V to needed voltages	2.1.011	all
LCM_OPTCON	Optical and electrical connections between main cable and LCM_CRATE	2.1.012	all
UNIV1	Daughter board plugged on other board for slow control MODBUS interface	2.1.013	all
BIDIANT	Daughter optical transceiver board for Ethernet and Clock signals	2.1.014	all
BIDITRIG	Daughter optical transceiver board for trigger signals	2.1.015	all
MLCM_DWDM	DWDM transceiver board with laser, receiver and DWDM filter	2.1.016	MLCM only
LCM_DAQ/SC	Data and slow control board which sends and receives Ethernet Protocol	2.1.017	all
MLCM_SWITCH	Gbit switch	2.1.018	MLCM only

List of references

http://antares.in2p3.fr/internal/deci-km2/tableaux/LCM and all references in that table, in particular technical note 3 LCM 20 01/A describing the LCM internal organisation

MasterLCM/SlaveLCM Test Bench

Schematic view of the LCM Test Bench



The Test Bench consists of a main computer connected with a set of instruments and devices. Each single board within the Design Under Test (DUT) is assumed to be already tested.

Specifications:

- The aim of the Test Bench is to test the overall functionality of SLCM/MLCM series production.
- The results of the tests must be logged in order to ensure *quality* documents.
- All the DUT communication links must be tested. These are:

    - Physical signals from OMs, LED ball and hydrophones;
    - 100 Mb Ethernet DAQ/SC optical link between Master and Slave LCMs;
    - 1 Gb Ethernet DAQ/SC optical link (only MLCM);
    - L1 and L2/RoR Trigger optical links;
    - Clock optical link.
- Test points inside the DUT must also be provided monitoring electrical parameters of interest.

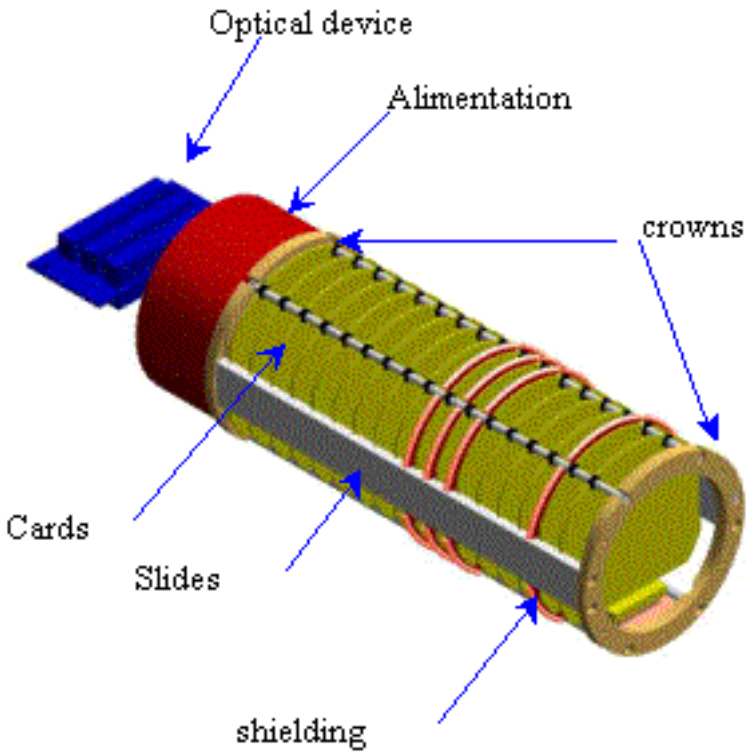
Interfaces with DUT are:

- LCM_TRIG board in order to test the L2 “2 storey” Trigger capability.
- LCM_DAQ/SC board for Master/Slave communication test.
- LCM_SWITCH board for Ethernet communications with Master LCM.

Technical Notes: 3 LCM 18 06 A LCM Test Bench

PBS 2.1.001 : LCM_CRATE(inside LCM container)

Schematic view of the inner rack



Description:

- The LCM_CRATE inner rack is housing the electronics embarked on the lines.
- It consists of an axial structure that links all the cards and the backplane
- Electric and optical cables penetrate the container and are plug in cards.
- This structure looks like a cylindrical cage placed inside the LCM container and fixed in the lower bottom end cap by a crown.

Dimensions, technological features:

- Effective inner diameter: 155 mm
- Effective inner length: 550 mm
- The selected material for all part of the inner rack is aluminium 2017. Both inner and outer diameters must be chamfered

Interfaces inside LCM are:

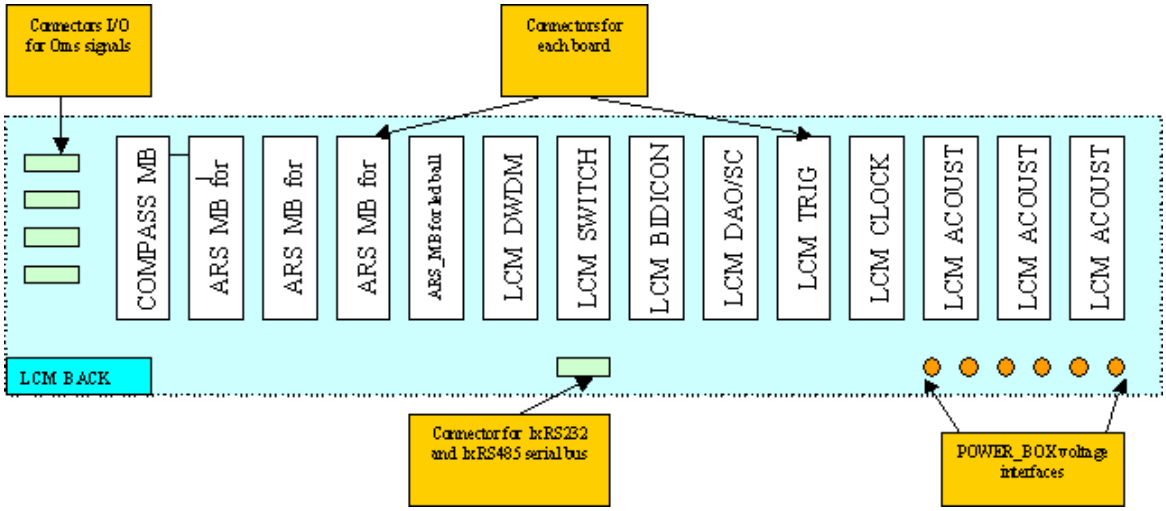
- 16 boards
- 1 electrical connection board
- 1 optical connection device
- LCM power box for voltage
- 4 shieldings for OEM and thermal conduction

Technical notes:

- 3 LCM 02 01:Integration LCM
- 3 LCM 02 03: shielding
- 3 LCM 02 04: crown 1
- 3 LCM 02 05: crown 2
- 3 LCM 02 06: Slides

PBS 2.1.002: LCM_BACK board (in LCM container)

Schematic diagramme of LCM_BACK board



The main functions of the LCM_BACK board are:

- Distribution, inside the LCM container, of all signals from or to each board inserted inside the LCM_CRATE.
- Distribution of electrical power (+5V, +3.3V, +2.5V, +1.8V, +12V, +48V) and common return, all these power signals come from the POWER_BOX fixed on the LCM_CRATE , which converts the 400V DC to all values needed inside the LCM.
- Interfaces between optical modules signals and the electronics boards (ARS_MB, POWER_BOX and COMPASS_MB).

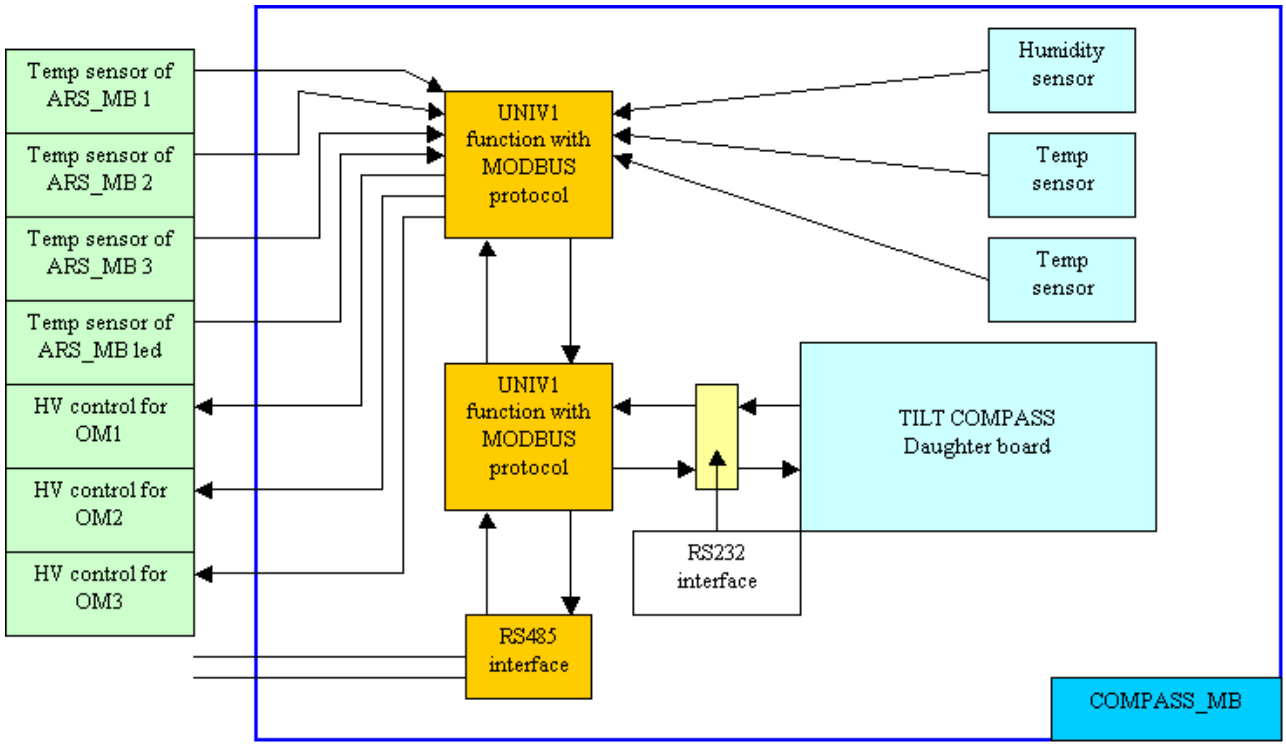
Interfaces inside the LCM are:

- Each board inserted in the LCM_CRATE is connected to the LCM_BACK by its rear connector (24, 48, or 96 pins). The location of each board is fixed in order to optimise parallel development and connections to the EMC.
- 4 connectors provide the interface with the optical modules and the LED beacon.
- 1 connector makes the interface with other containers for RS232 and the second RS485 serial bus, this connector provides the test signal for the LCM_DAQ/SC board (external test trigger signal). This connector drives also the main RS485 serial bus for all boards inserted inside the LCM_CRATE in order to test slow-control without the LCM_DAQ/SC board.
- The boards inserted inside the LCM_CRATE are (in the maximal configuration):

  COMPASS_MB, ARS_MB for OM1,2 and 3, ARS_MB for LED beacon, LCM_DWDM, LCM_SWITCH, MLCM_BIDICON, LCM_DAQ/SC, LCM_CLOCK, LCM_TRIG, LCM_ACOUST1,2 and 3 and POWER_BOX.

PBS 2.1.3 : COMPASS_MB board (in LCM and SCM containers

Schematic view of the COMPASS_MB board



The main specifications of the COMPASS_MB board are:

- Controls the Tilt compass daughter board with a RS485 MODBUS protocol and RS232 tilt compass daughter board bridge.
- Measures the humidity sensor which is included on the board for humidity control inside LCM and SCM containers.
- Measures temperature sensors (2 on the board)
- Reads the temperature sensors which are plugged on ARS_MB cards (1 temperature sensor for each ARS_MB : 3 sensors + 1 from ARS_MB LED if present).
- Controls the low voltage command of the high voltage of each optical module with 12 bits DAC with a 0 to 4 volts range (3 voltage commands).
- Measures the low voltage command value at the output of the DAC (3 voltage values)
- All these controls and measurements are performed through 2 UNIV1 functions with two different MODBUS addresses.

Interfaces inside LCM are:

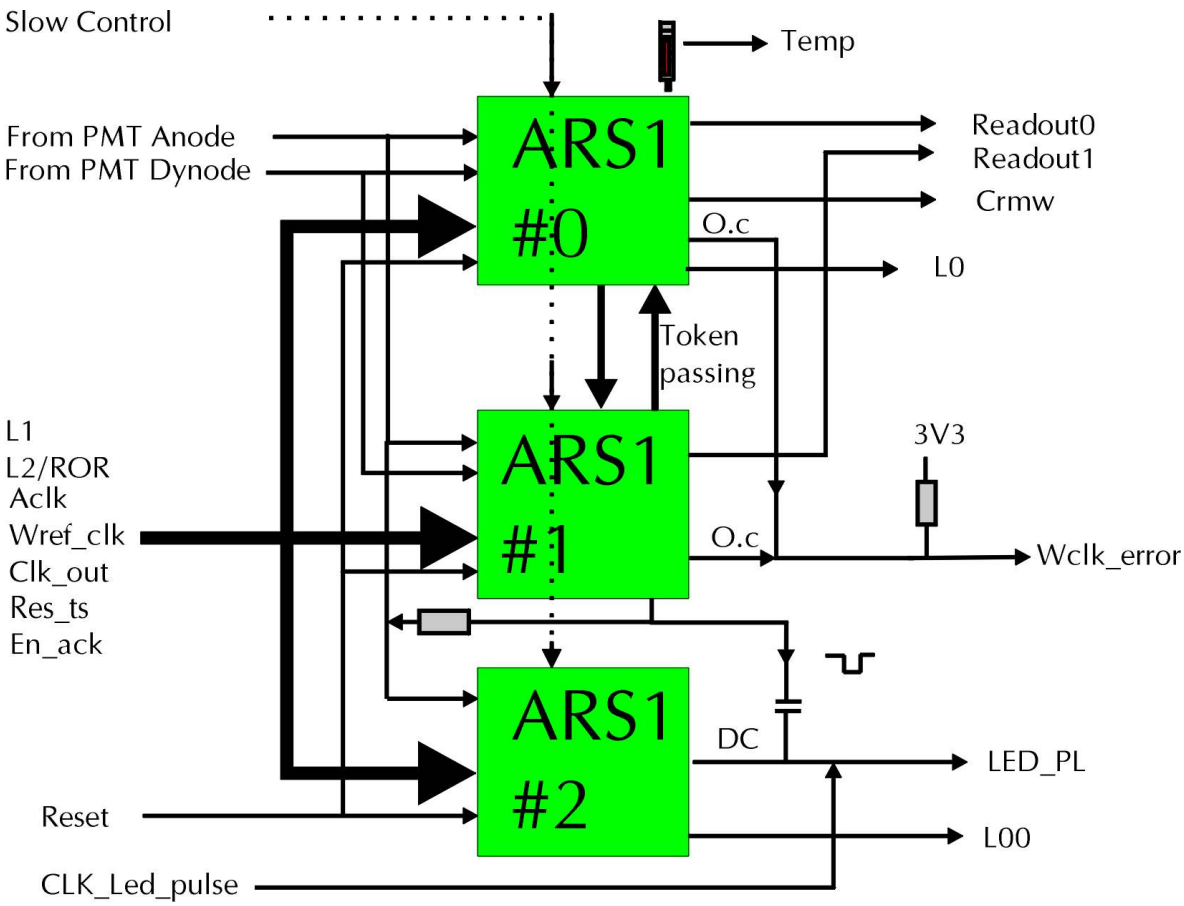
The standard interface is a 24 pins connector, all signals come from the backplane via the LCM_BACK board.

List of references

- 3LCM_07_01A : technical note of COMPASS_MB
- PBS 5.6 Humidity sensor
- PBS 5.2 Tilt meter and compass daughter board

PBS 2.1.004: ARS_MB board (in LCM/MLCM container)

Schematic of the ARS motherboard



The main functions of the ARS_MB board are:

- Interface of the 3 ARS chips to the LCM_DAQ/SC board. ARS#0 and ARS1#1 are used for signal processing, ARS#2 is used to generate of supplementary anode impulse trigger signal (L00) with its separate, slow control set, trigger level (th2)
- Passing of the token between ARS1#0 and ARS1#1
- Generation of LED pulser pulse and peak value reference voltage (0-24 V).
- Use of attenuated LED pulser pulse for re-injection in the anode for LCM tests without Optical Modules

Interfaces inside LCM:

- POWER BOX (~2W total): +48 V (2mA), +12 V (4mA), +6 V (160 mA), + 5 V(160mA), +5V(1mA), +3.3 V (250 mA), GND.
- LCM_TRIG: L0, L00, and L1, L2 (LVDS signals).
- LCM_CLOCK: ACLK, WREF_CLK (5 MHz), EN_ACK, RES_TS (LVDS signals), LED_PL (LVDS signals).
- LCM_DAQ/SC: CLK_OUT (40 MHz), READOUT1, READOUT0, CRMW (LVDS signals). ARS_RESET, SC_VALID, SC_CLK (CMOS/LVTTL signals), SC_DATA (bi-directional CMOS out, CMOS/LVTTL in), SC_OE (determines direction of SC_data for I/O buffer), WCLK_ERROR (open collector signal weakly pulled up to 5 volt on LCM_ARS board).
- COMPASS: ARS_COMPASS_temp (analogue)

Interfaces to OM:

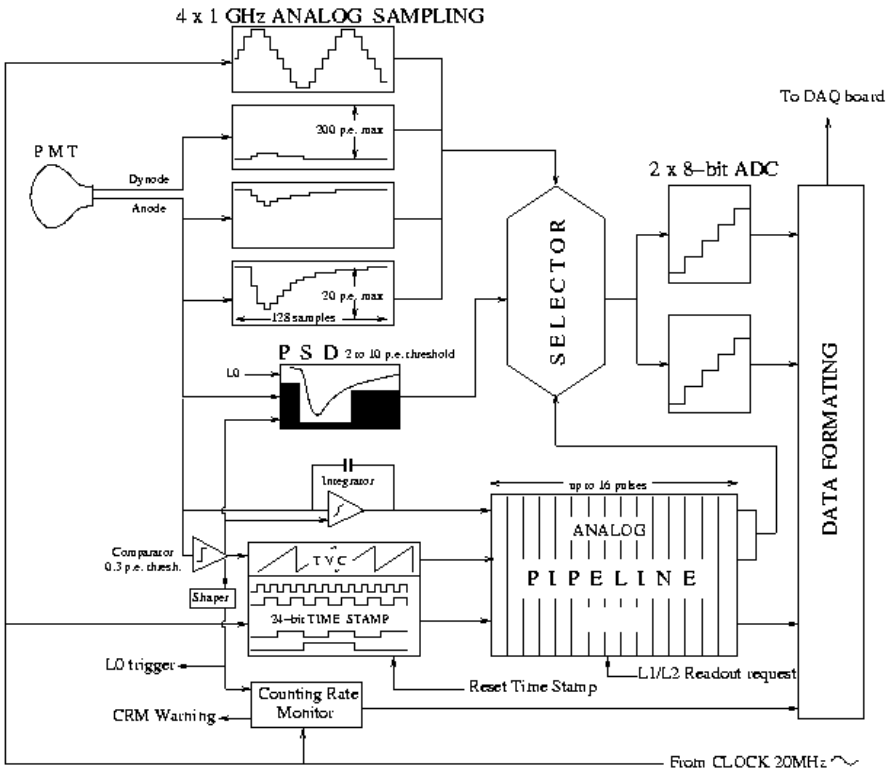
- LED_PL (twisted pairs) through back-plane connector.
- PMT anode and dynode signals via screened twisted pairs. there will be space at the far end of the backplane, where the incoming OM_LCM link will be connected to a cable going to the ARS_MB connector (type of connector MCX, type of cable RG178, 4 cables per ARS_MB).

Associated Technical Notes:

3 LCM 15 01 ARS motherboard

PBS 2.1.004.1: The Analogue Ring Sampler Chip (on ARS motherboard)

Schematic of the ARS signal processing



The Analogue Ring Sampling chip performs the off-shore processing of the PMT signals. It is located on the ARS motherboard of a LCM container.

The anode signal is sent to the comparator, the charge integrator, the Pulse Shape Discriminator, and the GHz waveform sampler. When a pulse exceeds the L0 trigger threshold of the comparator, its charge is integrated and the waveform is sampled while the PSD analyses the pulse shape and compares it to the predefined mask. At the end of the integration gate, the PSD returns the binary result whether the pulse is of the SPE type or the Waveform (WF) type. The timing of the signals is given by an external reference clock; the Time Stamp (TS) counts the reference clock pulses, and the Time-to-Voltage Converter (TVC) provides an analogue signal proportional to the time from the last clock signal to the instant when the pulse crossed the L0 threshold.

A pipeline memory is used to store the analogue and digital data. The pipeline consists of 16 memory cells to store up to 16 pulses. Each memory cell contains two analogue values (the integrated charge and the TVC) and 26 bits of digital data (the 24-bit Time Stamp, the 1-bit PSD result, and 1 bit to indicate if WF data has effectively been sampled). Once this information has been stored in the pipeline, the comparator, the integrator, and the TVC and Time Stamp functions are freed for the next pulse, without waiting for the digitisation of the pulses in the pipeline.

Waveform data is stored outside the pipeline. The GHz waveform sampler has four synchronous channels, sampling the reference clock, the anode signal, an attenuated anode signal, and a dynode signal. When a WF hit is found, the waveform sampling continues until 128 samples have been stored for each of the four fast-sampling channels; then the sampler is blocked until these data are digitised or discarded. If a WF event arrives when the WF sampler is occupied, the pulse will be treated as a SPE pulse with a flag indicating that the waveform sampler was not available.

The Time Stamp is used to determine if a pulse is in a trigger readout window. If a readout request is received, the memory cell is read out, the charge and the TVC are each converted to 8-bit digital values, and the digital information for the event, with a header added, is formatted for transmission to shore. For WF events, the 128 clock samples and the corresponding 128 anode pulse samples are converted to digital form and added to the event packet for transmission. For very large pulses, all four waveform channels are digitised : 128 samples each for the clock, the anode, the attenuated anode, and the dynode signals. If no readout request is received within a predefined lapse of time, the memory cell and the fast-sampling cells (in the case of a WF event) are erased and made available for subsequent pulses.

The main functions of the ARS chip are:

- Measurement of time of arrival and integrated charge of Single Photon Electron (SPE) PMT signals if confirmed by the trigger signals L1 or L2.
- Pulse shape discrimination (PSD) to separate SPE events from NON-SPE (waveform) events.
- Digitisation of waveform events measuring PMT anode, attenuated anode and dynode signals as well as the sinusoidal time reference clock (band filtered ACLK clock signal).
- Generation of L0 signal when PMT anode signal crosses threshold th1.
- Generation of Counting Rate Monitor Warning (CRMW) signal set to go off at a determined PMT pulse rate.
- Generation of WCLK_ERROR if the waveform digitizer Delay Locked loop (DLL) is unlocked.

ARS Specifications:

Parameter	Min spec.	Max spec.	Expected value	Characteristics
V_{sup}	4.75 V	5.25 V	5 V	Operating power supplies range.
D_{sup}		+/-25 mV		Power supplies drift, other than ADC.
D_{supadc}		+/-1 mV		ADC power supply drift (vdd_adc).
T	0°C	50°C	15°C	Operating temperature.
D_T		+/-3°C		Temperature drift.
P_{sup}		250 mW	200 mW	Power consumption of the ARS1 5-V supplies.
Fs	300 MHz	1 GHz		Waveform mode sampling frequency.
Nc	4			Number of Waveform mode channels : *anode*, two intermediate gain channels (*dynodes*), *and Aclk* clock.
Ns	128			Number of Waveform mode samples per ARS1.
N_{ARS}	1	4	2	Number of ARS1 chips in the token ring.
V_{SPE}			60 mV (13 pC)	Single photoelectron pulse amplitude at the ARS1 input.
D_{add}	1.5 V		3.5 V	Dynamic range of the *anode, dynode1* and *dynode2* Waveform mode inputs.

D_{aclk}	2 V		3.5 V	Dynamic range of the *Aclk* input.
Gw	0.9		1.0	Waveform mode gain.
Lw		5 %	2 %	Integral linearity of the Waveform mode.
Dq	10 PE		13 PE	Dynamic range of the *anode* input for charge measurement (SPE mode).
G_{SPE}	7.3 mV/pC			Charge integrator transfer function.
L_{SPE}		5 %	2 %	Integral linearity of the integrator.
N_{add}		5 mV RMS	3 mV RMS	Total noise at the Waveform mode inputs.
Nq		0.5 pC RMS		Total noise at the SPE mode input.
BW	120 MHz		140 MHz	Bandwidth of the Waveform mode inputs (-3dB).
Ci	5 pF	40 pF		Analogue input capacitance. The maximum value is the worst case-operating mode of the ARS1.
Ri	25 Ω	50 Ω		Expected resistance at the analogue inputs (Thévenin equivalent resistance).
F_{aclk}	10 MHz	20 MHz		*Aclk* clock frequency. Notice : this frequency must be Fs/64, when *Aclk* is used as the reference-sampling clock.
F_{RO}	15 MHz	25 MHz	20 MHz	Readout clock frequency. This clock divided by two, is used as the ADC clock.
N_{ADC}			8 bits	Dynamic range of the ADC.
Neff	7 bits			Effective number of ADC bits, for a LSB of 6 mV.
S_{TVC}	20 mV/ns	120 mV/ns	50 mV/ns	TVC conversion linear slope.
L_{TVC}		5 %		Integral linearity of the TVC.
N_{TVC}		400 ps RMS		Equivalent noise of the TVC.
DS_{TVC}			4.3 ps/mV	TVC drift as a function of power supply (5 V).
DT_{TVC}			33 ps/°C	TVC drift as a function of temperature.
N_{TS}			24 bits	Dynamic range of the Time Stamp.
Tw_{min}	12 ns	70 ns		Minimum L0 trigger pulse width. The maximum pulse width is $4.Tw_{min}$.
Vth_{L0}	15 mV		5 mV	Minimum L0 trigger threshold.
$DVth_{L0}$		20 %		Threshold accuracy, including drift.
Tb_{T1}	20 ns	100 ns	$0<Tb_{T1}<200$ ns	Return timing of the L1 trigger.
Tb_{T2}	1 µ s	35 µ s		Return timing of the L2 trigger.

Links to ARS event formats

- STATUS event
- RTS event
- CRM event
- SPE event
- WAVEFORM event
- WAVEFORM+DYNODES event

Link to ARS Slow control parameters

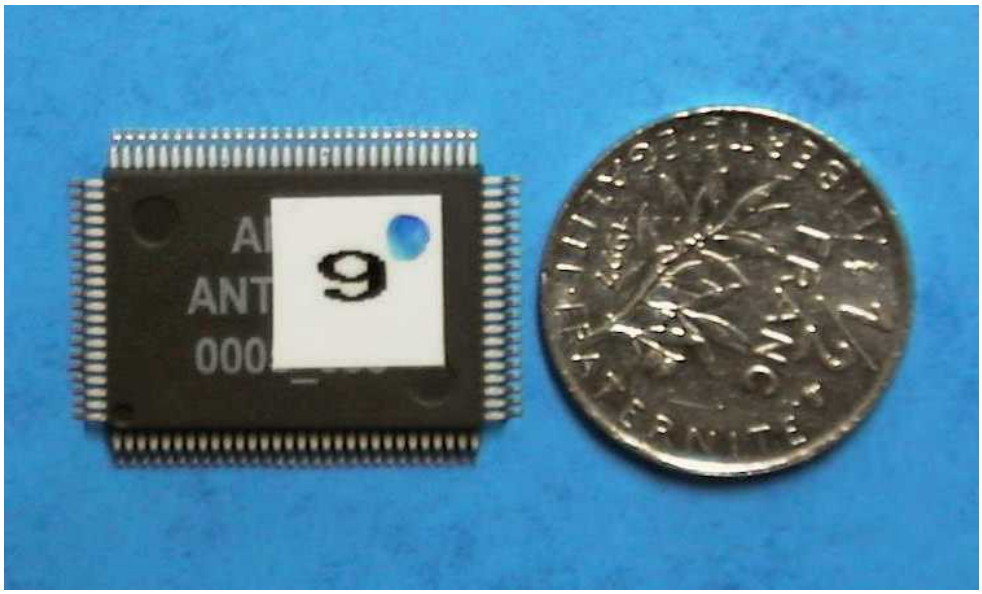


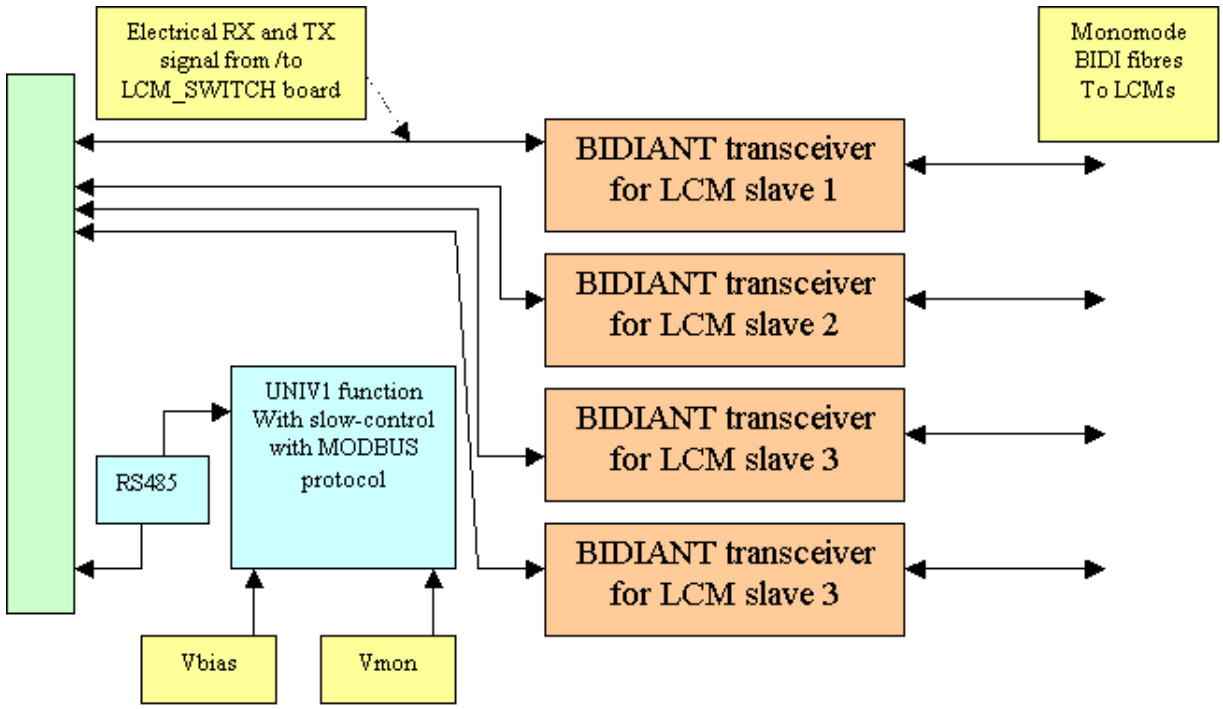
Photo of the ARS chip

Associated Technical Notes:

- 3 LCM 15 01/C ARS motherboard
- Elec/2000-6 ARS1 Analogue Ring Sampler (and ARS_CONV) Users Manual V1.9
- ARS results for physicists

PBS 2.1.005: MLCM_BIDICON board (in Master LCM container)

Schematic diagramme of the LCM_BIDICON board:


Electrical RX and TX signal from /to LCM_SWITCH board
Monomode BIDI fibres To LCMs
BIDIANT transceiver for LCM slave 1
BIDIANT transceiver for LCM slave 2
BIDIANT transceiver for LCM slave 3
BIDIANT transceiver for LCM slave 3
UNIV1 function With slow-control with MODBUS protocol
RS485
Vbias
Vmon

The main functions of the MLCM_BIDICON board are:

- Concentration of Ethernet channels from each LCM slaves of one sector.
- Optical/electrical conversion with BIDIANT daughters boards transceivers (4 boards, one for each LCM slave container)
- Monitoring of the Voltage of each BIDIANT daughter board.
- Slow-control interface with standard MODBUS protocol via the UNIV1 daughter board.

Interfaces inside LCM are:

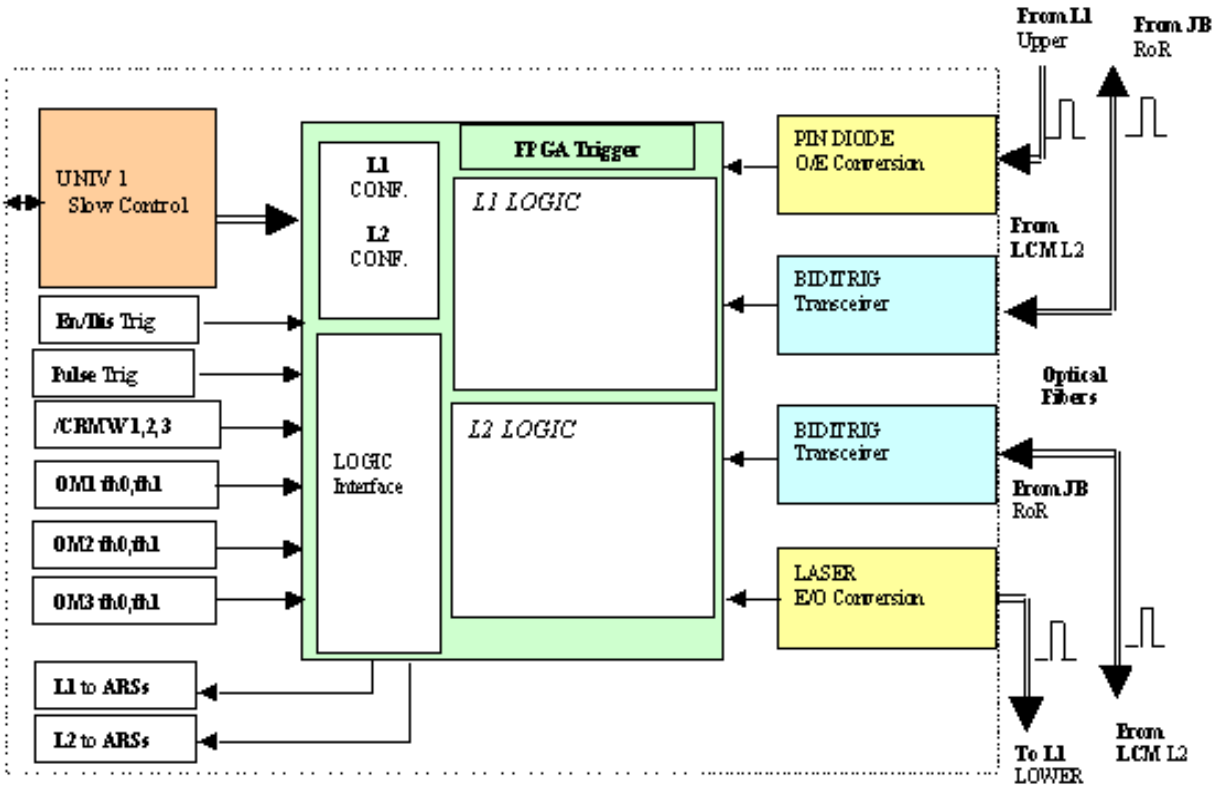
- LCM_DAQ/SC board for clock signal, reset/enable and Slow Control RS485 bus by twisted pairs on backplane.
- MLCM_SWITCH board with twisted pairs PECL (RX and TX signal) on backplane.
- POWER_BOX for voltage (+5V and +3.3V) from backplane

Associated Technical Notes:

- 3 LCM08 04: BIDIANT/BIDIDEV User's manual
- 3 LCM08 01: UNIV1 User's manual
- 3 LCM20 01: LCM internal organisation.

PBS2.1.006: LCM_TRIG (in LCM container)

Schematic diagramme of the LCM_TRIG board:



The main functions of the LCM_module are:

- Reduce rate and size of data to that manageable by the DAQ system and the ONSHORE filter
- Generate a L1 trigger for local readout of the LCM.
- Generate a L2 trigger for global readout of the whole detector.
- A variety of options for the L1 and L2 trigger requirements, based on coincidences between th0, th1 signals of the local storey and the L1 trigger from the upper storey.
- Delays, pulse widths configured by slow control via UNIV board, precision of 10ns.
- BIDITRIG daughter board used to receive/transmit L2 and RoR on single fibre.

Interfaces to :

- LCM_DAQ/SC board by slow control RS485 bus by twisted pairs on backplane.
- ARS boards (1-2-3-4) by twisted pairs for: Trigger 0 – 00 - L1 – L2, RoR signals.

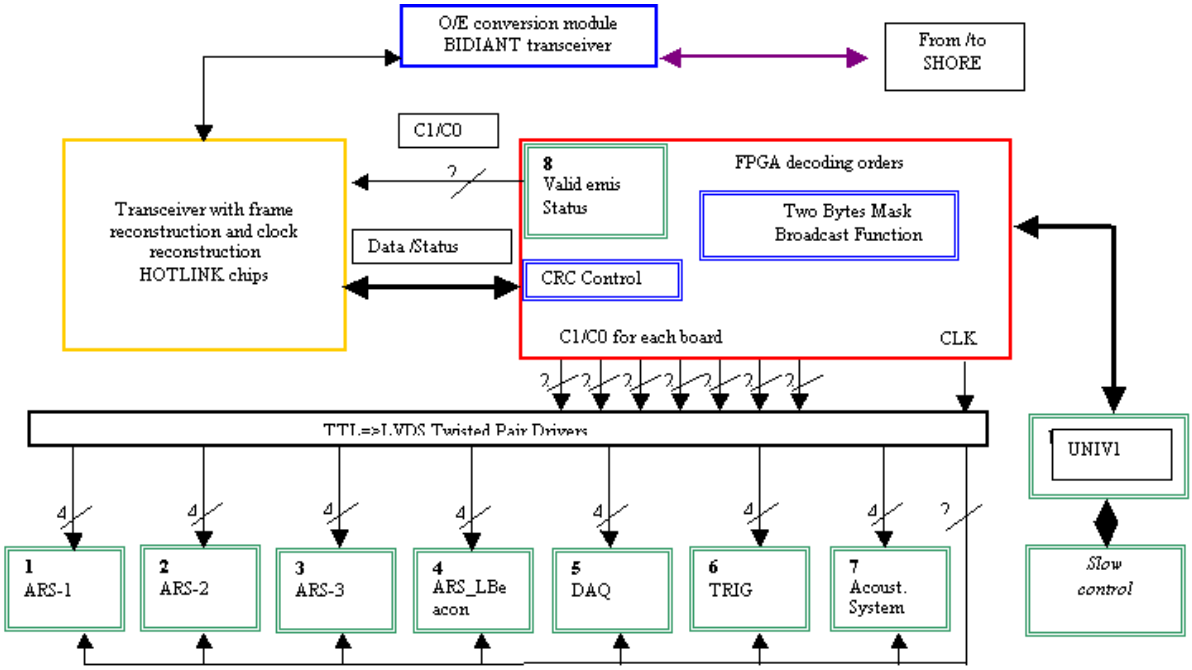
- JB (Junction Box): L2 /RoR optical signals for accept event.
- LCM_DAQ/SC board: L1, L2, RoR information for monitoring purposes.
- LCM_CLOCK board: for clock signal, Enable/Disable Trigger, Pulse_Trig signals.
- CRMW: Continuous Rating Monitor Warning signal from ARS boards.
- LCM upper/lower: via Optical fibres for L1- L2 – RoR signals propagation.

Associated Technical Notes:

- ANTARES-Elec/2000-07 " *Level 1 Level 2 Offshore trigger* "
- 3 LCM 06 01: Trigger Board Interfaces Description
- 3 LCM 20 01: LCM internal organisation (a proposal)
- 3 LCM 03 02: Clock Board interfaces description

PBS 2.1.007: LCM_CLOCK board (in LCM container)

Schematics of the LCM_Clock board



The main functions of the LCM_CLOCK board are:

- Distribution inside the LCM of the onshore reference clock (20 MHz) to all boards which used this signal for the time stamp or command functions.
- Generation of synchronous commands, via lines on the backplane, for ARS (Enable/Reset), DAQ (Enable/Reset), acoustic positioning system (low rate and high reset), Trigger (Enable/window pulse).
- Return path possibility in order to read status byte from a specific LCM to shore station.
- Slow control parameters reading for board monitoring, with UNIV1 daughter board. The main parameters are: optical signal detection, temperature measurement, laser bias current and modulation, byte status, filter addressing mask configuration etc..

Interfaces inside LCM:

- LCM_DAQ/SC board for clock signal, reset/enable and slow_control RS485 bus by twisted pairs on backplane
- Trigger board (LCM_TRIG) clock signal and enable/pulse twisted pairs on backplane
- Acoustic boards (ACOUST_RX_PREAMP, ACOUST_RX_DSP and ACOUST_RX_DSP) for clock signal, and resets by twisted pairs on backplane.
- ARS_MB for clock signal and reset time stamp by twisted pairs on backplane.

- ARS LED beacon for clock signal and reset by twisted pair on backplane.
- LCM power box for voltage (+5V and +3.3V) by backplane.
- LCM optical connection board (LCM_OPTCON), via the BIDIANT transceiver, to the main cable.

Associated Technical Notes:

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 03 02: Clock Board interfaces description
- 3 LCM 18 02: Clock distribution prototypes tests

PBS2.1.011: Power Box for LCM and SCM

The LCM power module is contained within a copper housing, which is mounted at one end of the power and data bus support assembly. To minimise EMC radiation, all input and output electrical connections are made through individual ceramic filters and the housing lid is sealed with beryllium-copper finger strips.

The power module is based upon a VICOR second generation DC to DC converter capable of operating with an input voltage range of 290 to 450 V. The first converter generates an internal supply of 48 V, which is used as the power input to all other converters within the module.

The SCM Power Supply is a copy of the LCM POWER_BOX, although less voltages are used in the SCM.

Output Specifications

OUTPUT VOLTAGE in Volts	MAXIMUM POWER in watts	EFFICIENCY in %
48	50	85
48 switched outputs	3.0 per channel	85
12	3.0	71
5.5	15	70
5.0	50	72
3.3	50	72
2.5	8.0	64
1.8	see below	44

General remarks

a. All outputs (with the exception of the 1.8-volt supply) are fully isolated and there is no common connection within the power unit. The 1.8-volt supply is derived from the 2.5-volt output and therefore the two supplies share the total power (8 watts).

b. The maximum power quoted in the above table **does not** imply that this level of power is available for general use. It is the maximum capability of the individual converters under ideal conditions. The available power will depend upon, load distribution, efficiency and most importantly the **thermal characteristics** of the LCM.

c. The efficiency quoted, is the overall value from the 400-volt input to the particular output (the efficiency is not constant with load and the above figures are only representative)

d. Final values for the noise output from each supply will be given when the new prototype module is tested.

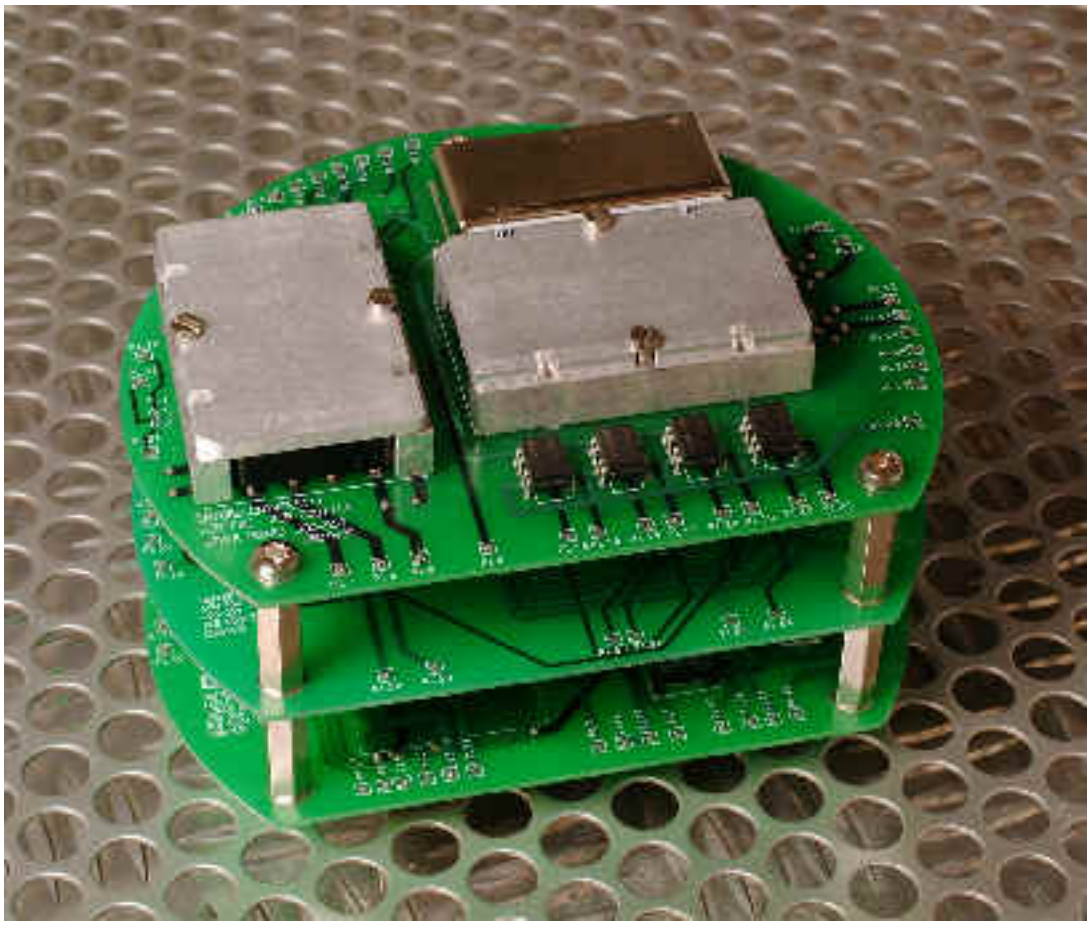
Detailed view of the electrical layout of the power module

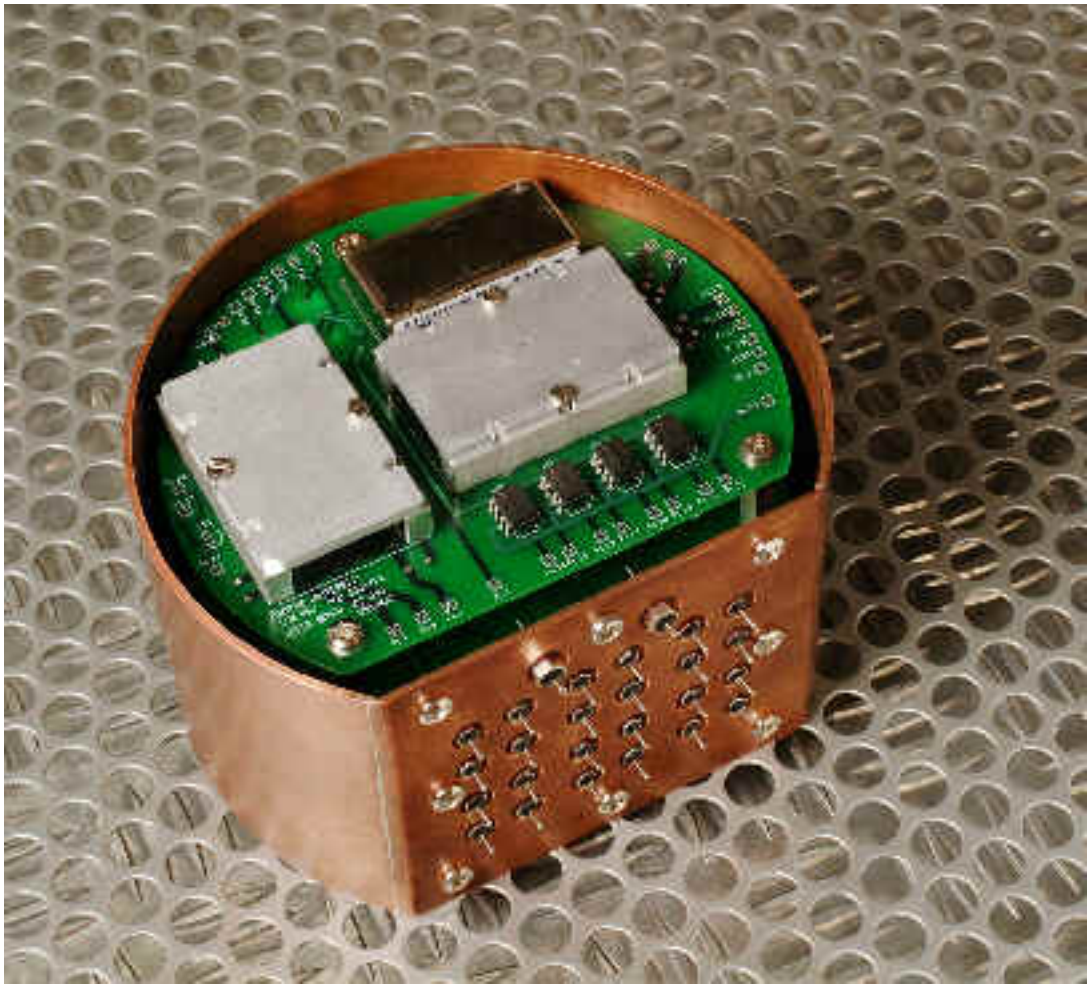
Slow Control

The slow control has only two functions:

1. Monitoring all output supplies (voltage and current) and the internal temperature of the module.
2. Operating the optical switches, which isolate the OM power under fault conditions.

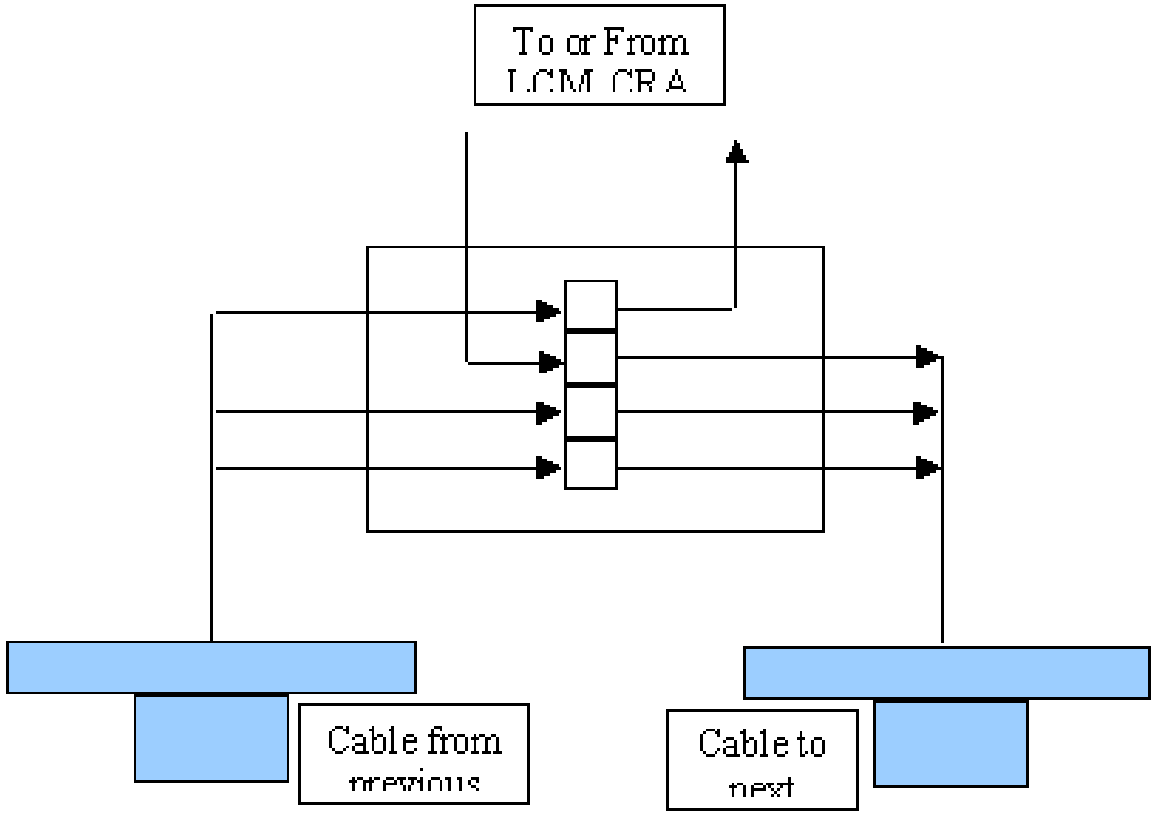
Physical views of the LCM Power_Box





PBS 2.1.012: LCM_OPTCON board (in LCM container)

Schematic of the LCM_OPTCON board



The main function of the LCM_OPTCON board is the distribution of all optical fibres or power wires from the EMC to the LCM_CRATE boards or pass them to next floor.

Each cable (penetrator) has 21 optical monomode fibers and 9 power wires. The LCM_OPTCON board includes optical connectors and solder contact points for signal distributions.

Optical connectors are OPTOCLIP II connectors from Deutsch company, these connectors has been tested with a power loss insertion lower than 0.1 dB and reproducibility better than 0.05 dB.

For electrical power connection, each LCM_OPTCON board includes PCB wire configuration which can be cut or assign for each floor before integration

The LCM_OPTCON board is fixed to the upper flange of the LCM container.

Interfaces inside LCM are:

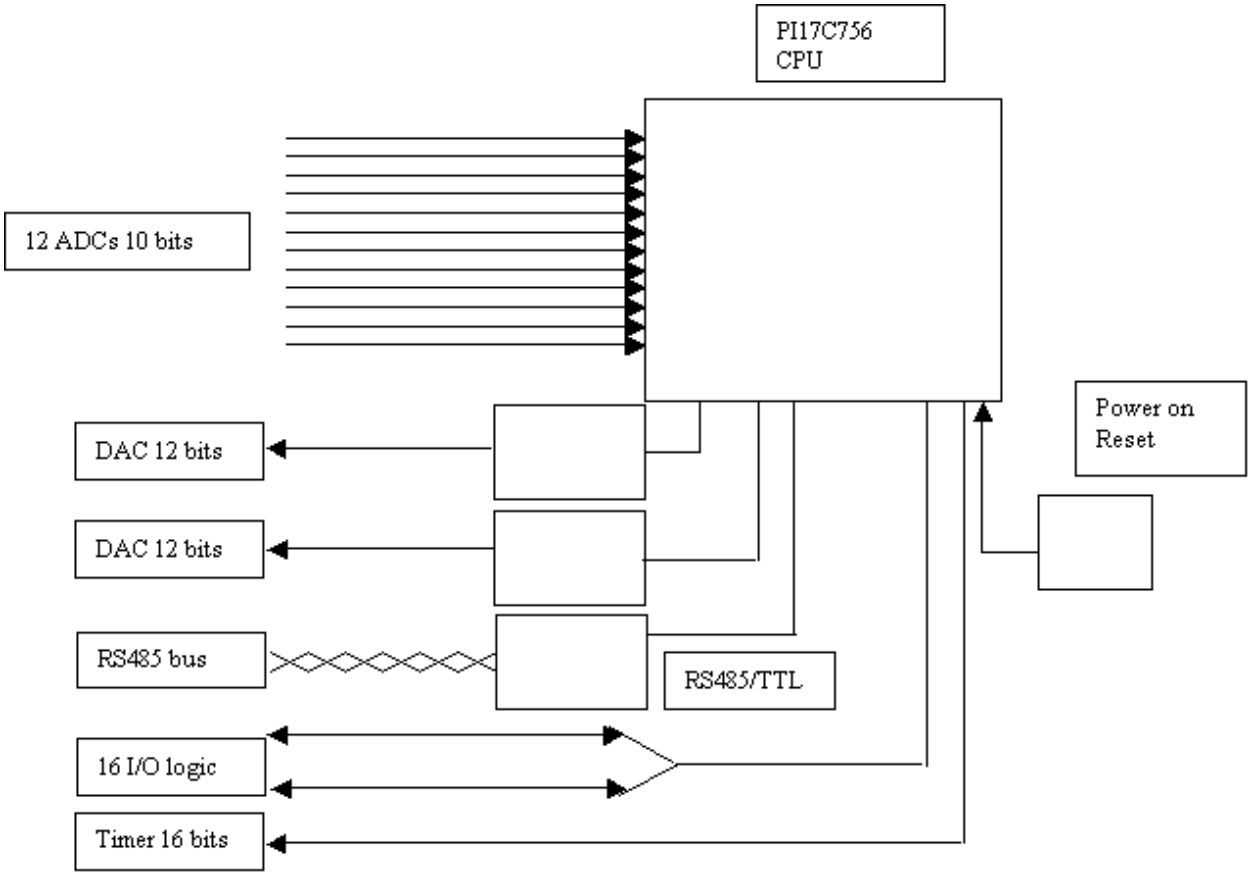
- Maximum needs for optical connectors : 27; 30 OPTOCLIP II connectors are available.
- Maximum needs for optical fibers with LCM_CRATE boards: 9 for Master LCM and 2

wires for 400V.

OPTCON prototype board picture

PBS 2.1.013: UNIV1 board (in LCM, SCM, JB containers)

Schematic diagramme of the UNIV1 board



The main functions of UNIV1 board are:

- Main hardware interface between the DAQ/SC board and the setting and reading of the Slow-Control parameters of each board inserted in the containers.
- MODBUS protocol in micro-controller with RTU format.
- 10/12 Analog to Digital converters with 10 bits of precision.
- 2 Digital to Analog converters with 12 bits of precision.
- 16 digital pin selectable individual y in IN or OUT state.
- 1 timer with 16 bit range, second serial bus with buffer transmission and reception.

Interfaces inside LCM, SCM and JB are:

- The UNIV1 board is a daughter board which drives all slow-control functions for its main board. Hardware adaptation are very small or not necessary.

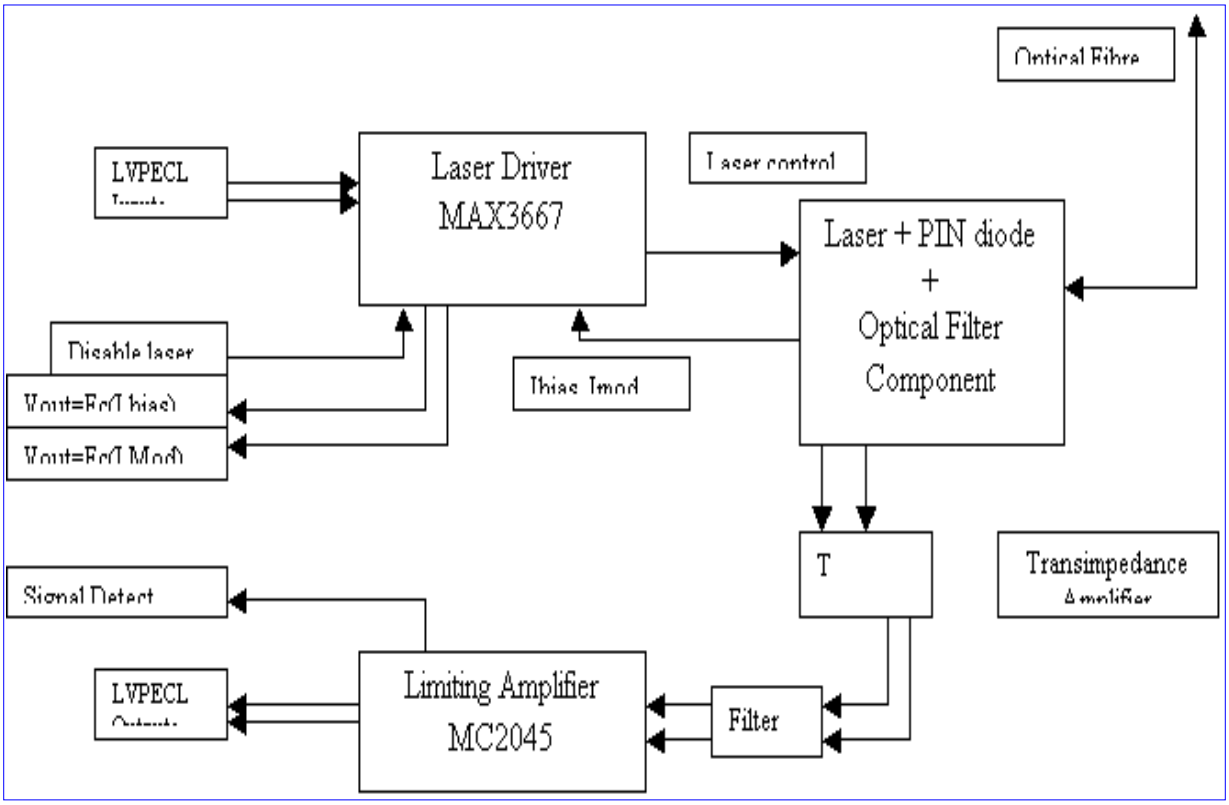
Picture of the UNIV1 Board

Associated Technical Notes:

- 3 LCM 08 01/A : UNIV1 user's manual
- 3 LCM 08 02/A: MODBUS reference guide

PBS 2.1.014: BIDIANT board (in LCM container and SCM container)

Schematic diagramme of the BIDIANT transceiver



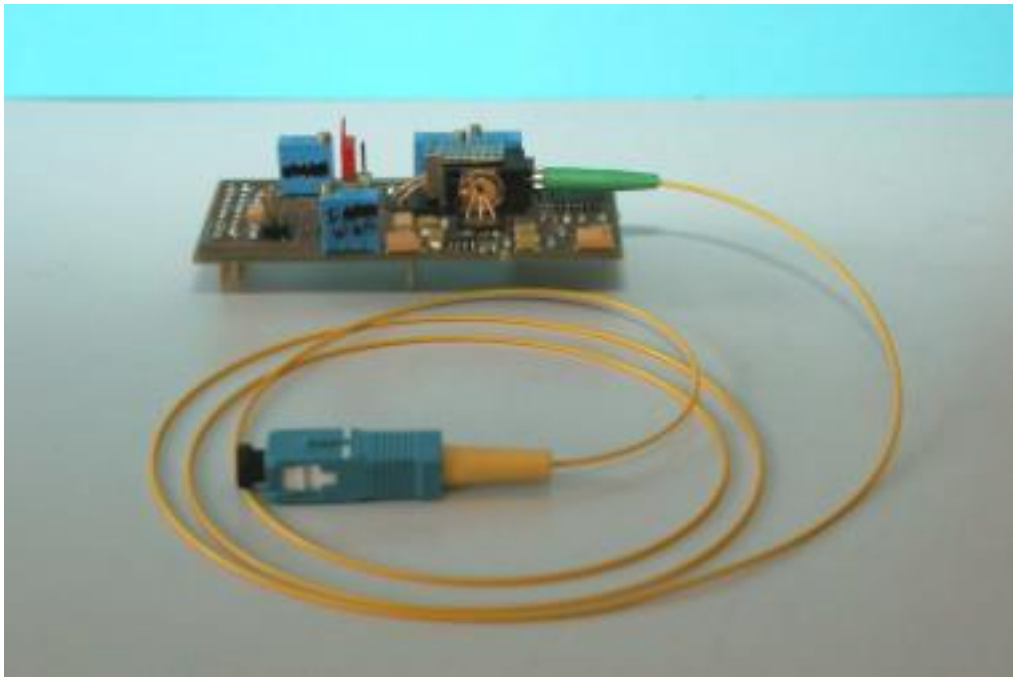
The main specifications of the BIDIANT transceiver board are:

- Bidirectional distribution of Ethernet or clock distribution using only one optical fibre
- Ethernet transmission between LCM slaves and LCM master inside sector, with 1310/1310 nm bi-directional capability.
- Clock distribution inside sector, with 1310/1550 nm for LCM and 1550/1310nm for SCM containers.
- Modulation current between 5 to 60 mA with a maximum optical power of –3 dBm for laser diode.
- Laser diode current between 5 to 30 mA with APC power control.
- Receiver part with transimpedance and limiting amplifier, with a sensitivity better than –23 dBm for 1310/1550 nm and –20 dBm for 1310/1310 nm.
- Each transceiver board produce voltages to allow monitoring of the laser diode modulation and bias current. These parameters can be read by the Slow-Control of the UNIV1 board

- Inputs and Outputs are differential in LVPECL format.
- Signal detection permits to detect optical power at the receiver.

Interfaces inside LCM:

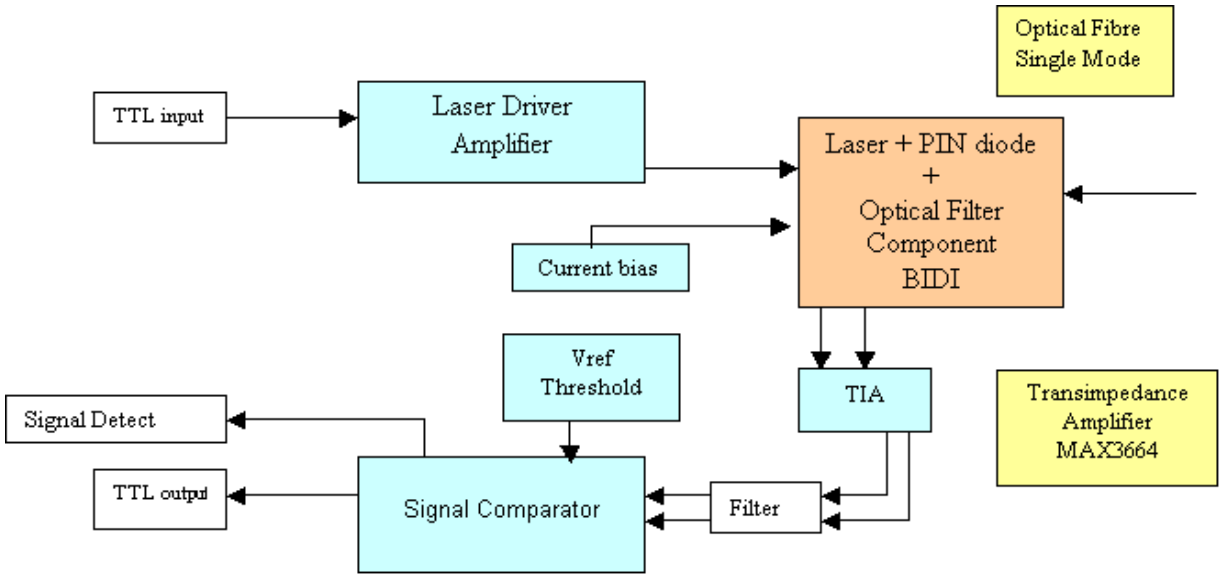
- The BIDIANT transceivers are standard 2x9 pinout, with additional pin for PIN diode bias voltage (Between 3 to 10 Volts max)
- Optical fibres are mounted with OPTOCLIP II connectors.



Picture of the BIDIANT board

PBS 2.1.015: BIDITRIG board (in LCM container and JB containers)

Schematic diagramme of the BIDITRIG transceiver board



This board is a daughter board which is plugged on the LCM_TRIG and JB_TRIG boards. An example of a BIDITRIG board implementation can be seen with the picture of the BIDIANT board, the external aspect is similar.

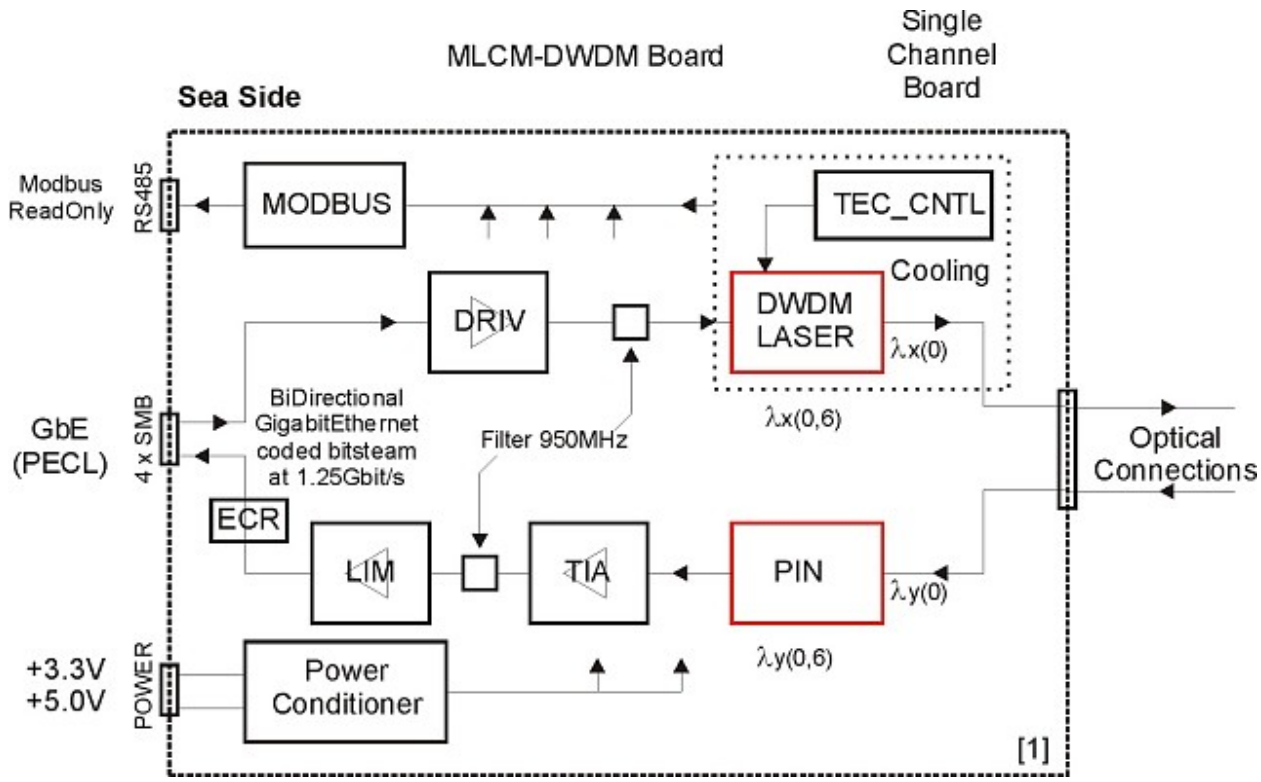
The main functions of the BIDITRIG transceiver board is the electrical/optical conversion between TTL pulse of trigger signals L2 and RoR and monomode optical fibres inside the line cable.

Interfaces inside LCM and JB are:

- The BIDITRIG daughter board has standard TTL input and output. Power needed +5 V.
- Like the BIDIANT daughter board, the BIDITRIG incorporates standard BIDI component with pigtail and standard OPTOCLIP II connector on the optical fibres.

PBS 2.1.016: MLCM-DWDM Board (in MLCM container)

Block diagramme of the MLCM-DWDM Board



The MLCM-DWDM Board converts the Gigabit ethernet signals from the LCM_SWITCH Board into the optical signals of a Dense Wavelength Division Multiplexing (DWDM) system and vise versa. Important parts on this board are the DWDM Laser and the Pin-Diode Receiver.

The DWDM Laser is a Distributed Feedback type with very narrow spectral width, operating in the 1550nm range at 1.25 Gb/s. The system is based on the ITU grid standards for DWDM applications with 400 GHz channel spacing. The specific optical ITU-channel wavelength λ_x is obtained by very accurate temperature control with a Thermo-Electric Cooler (TEC).

Temperature stabilisation of < 0.1°C is needed for 0.1 nm wavelength locking. The Pin-Diode Receiver with Trans Impedance Amplifier (TIA) and Limiting Amplifier (LIM) converts the optical signal λ_y back to an electrical signal.

The main functions of MLCM-DWDM Board are:

- Electro-optical conversion and vise versa of Gigabit Ethernet 1000BASE-CX signals.
- DWDM laser temperature control to < 0.1°C.
- Slow control parameters read-only for board monitoring, with UNIV1 daughter board. The main parameters are: optical signal detection, laser temperature measurement, laser

wavelength lock, laser bias current and laser modulation current.

Interfaces inside MLCM are:

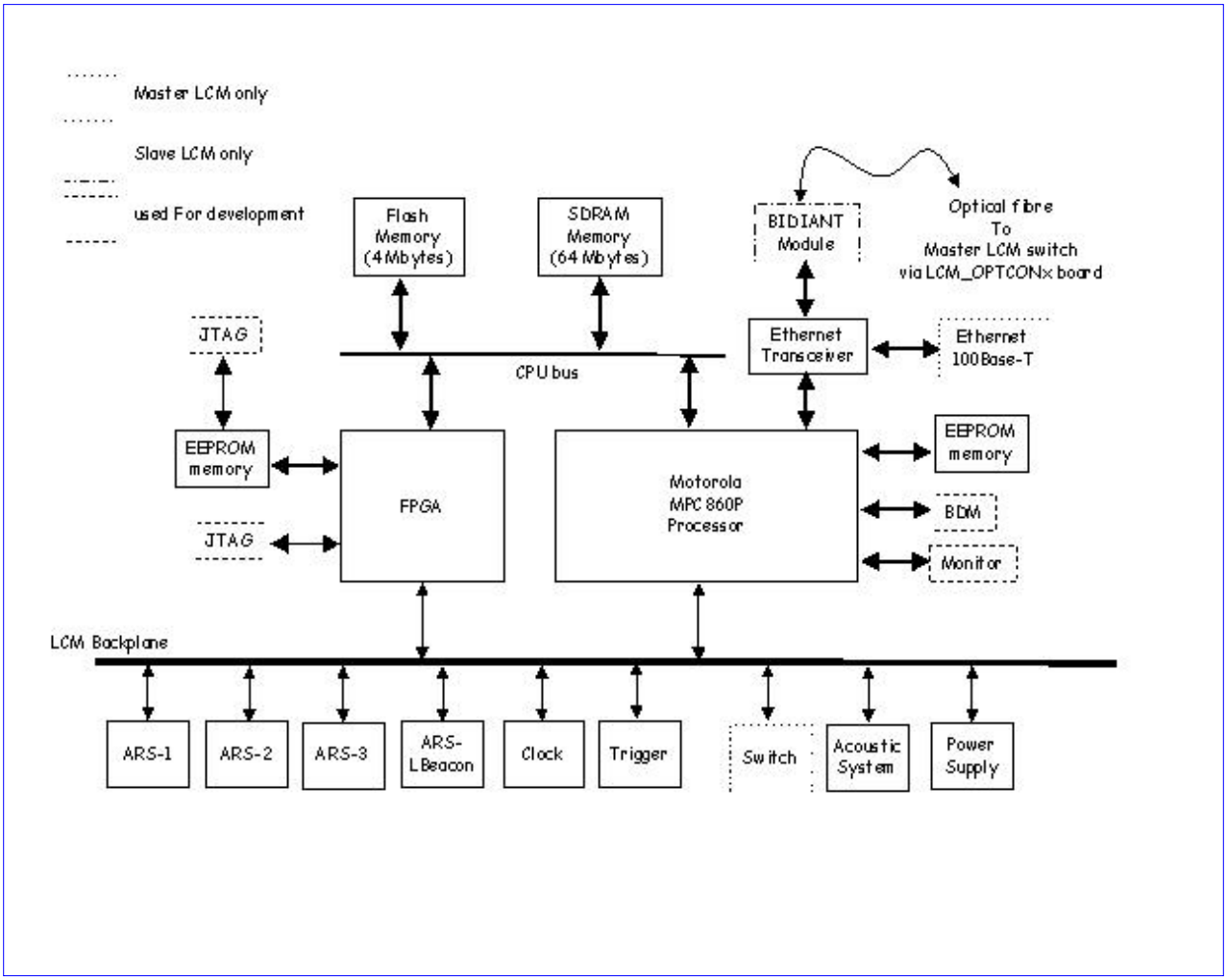
- DAQ/SC Board for Slow-Control, RS485 bus by twisted pairs on LCM backplane.
- MLCM_SWITCH board signals via coaxial SMB connectors.
- Optical I/O via the EMC to the SCM-DWDM-MUX & DEMUX.
- Backplane for supply Voltages: 3.3V and 5.0V.

Associated Technical Notes:

- http://www.nikhef.nl/~n05/antares/ETR_Notes/ETR2000-07s.pdf
- http://www.nikhef.nl/~n05/antares/ETR_Notes/ETR2000-08s.pdf

PBS 2.1.017: LCM_DAQ_SC board (in LCM container)

Schematic diagramme of the LCM_DAQ_SC board



The main functions of the LCM_DAQ_SC board are:

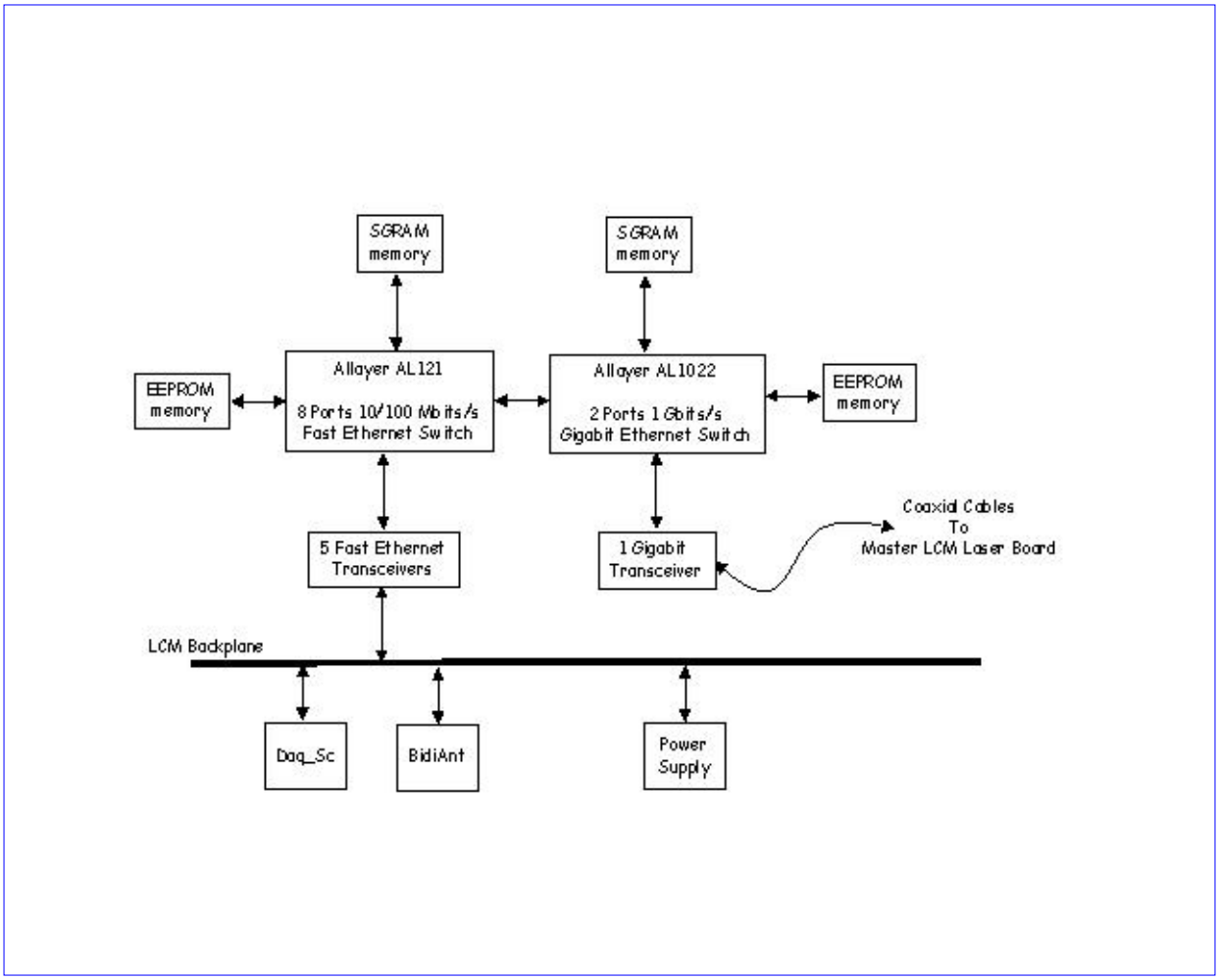
- Readout of the data produced by the ARS.
- Transmission of the resulting data through the line network.
- Processing of slow control data and commands.
- Possible transmission of trigger data: special packets –issued with each trigger– containing the trigger time and geographical origin.
- Extend the ARS event time-stamp to 32 bits.

Interfaces inside LCM are:

- Clock board (LCM_CLOCK) for clock signal, reset/enable DAQ and Slow-Control over Modbus Protocol.
- Trigger board (LCM_TRIG) for Readout Request, L2 and L1 trigger signals.
- Acoustic boards (ACOUST_RX_PREAMP, ACOUST_RX_DSP and ACOUST_RX_CPU) for slow-control over Modbus Protocol.
- ARS motherboards (ARS_MB) for data readout and Slow-control. Both slow-control and readout are carried by the DAQ FPGA over the ARS protocol.
- LCM power box for voltage (+3.3V and +1.8V).
- LCM optical connection board (LCM_OPTCON), via the BIDIANT transceiver daughter board, in order to connect optical signals to the main cable.

PBS 2.1.018: MLCM_SWITCH board (in Master LCM container)

Schematic of the MLCM_SWITCH board



The main functions of the MLCM_SWITCH board are:

- Merge all Ethernet link (100 Mbits/s) coming from the LCM_DAQ_SC boards of a sector into a single Ethernet link connected to the DWDM laser board (1 Gbits/s).
- Common link characteristics : Ethernet protocol, bi-directional and full-duplex.
- Configured at power-up.

Interfaces inside LCM are:

- Master LCM BIDIANT board. The BIDIANT transceivers, which receive the link coming from all the LCM_DAQ_SC boards of a sector are connected to 4 Fast Ethernet transceivers

via PECL signals over the backplane.

- MLCM_DWDM for the Gigabit link over coaxial cables.
- LCM power box for power (+3.3V and +2.5V)
- The local LCM_DAQ_SC board

PBS2.2: The String Control Module (SCM)

The String Control Module (SCM) contains the electronics concerning the Slow Control, clock, and instruments for acoustic positioning and sea properties.

The SCM container is similar to the LCM container and is located in the Botttom String Socket (BSS). It is coupled to the String Power Module (SPM).

The individual cards in the SCM have dedicated test benches, as is the case for the LCM cards. The tests foreseen for the SCMs are summarised in the page on Integrated SCM test benches.

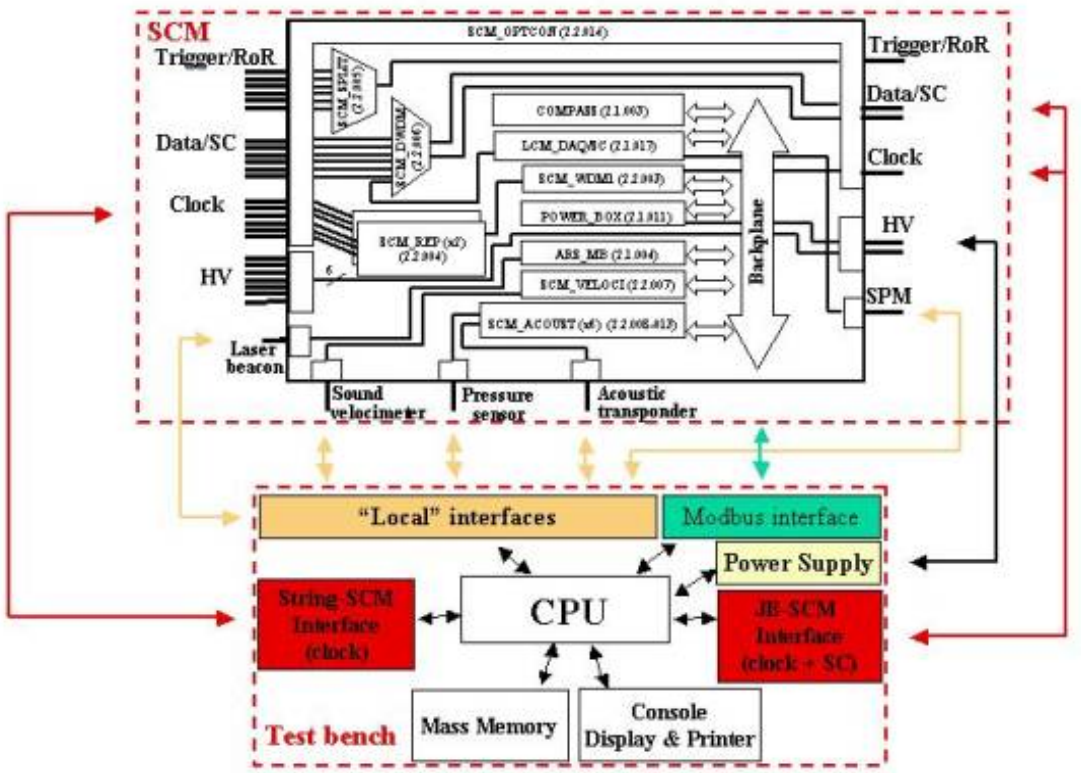
Components in a SCM

Objects in SCM	Description	PBS number
SCM container	Titanium container	1.2.006
SCM_CRATE	support of boards and backplane	2.2.001
SCM_BACK1	distributes signals between boards in SCM_CRATE	2.2.002
SCM_WDM1	optical transceiver WDM with clock distribution	2.2.003
SCM_REP	optical transceiver to regenerate clock signal	2.2.004
SCM_CLOCK	Clock distribution for SCM	2.2.005
SCM_DWDM	Optical transceiver for DWDM function with laser and receiver part	2.2.006
ACOUST_RXTX_EM	Positioning system	2.2.007
ACOUST_RXTX_PREAMP	Positioning system	2.2.008
ACOUST_RXTX_DSP2	Positioning system	2.2.009
ACOUST_RXTX_DSP1	Positioning system	2.2.010
ACOUST_CPU	Positioning system	2.2.011
ACOUST_POW	Positioning system	2.2.012
SCM_OPTCON	Optical connections between main cable and SCM_CRATE	2.2.013

SCM_DWDM_ MUX/DEMUX	Optical mux and demux to separate or mix wavelengths from shore or Master LCM	2.2.014
COMPASS_MB	Controls and measures tiltmeters, humidity and temperature sensors (id. LCM)	2.1.003
ARS_MB	analog pipeline with ADC conversion from PMT signal (identical to LCM)	2.1.004
POWER_BOX	Converts 400V to needed voltages (id. LCM)	2.1.012
UNIV1	Daughter board plugged on other board for slow control MODBUS interface	2.1.013
LCM_DAQ/SC	Data and slow control board which sends and receives Ethernet Protocol	2.1.017

SCM Test Bench

SCM Test Bench synoptic



Specifications:

The SCM Test Bench will have to certify the full functionality of the SCM. It will do so by checking that:

- the SCM correctly executes the SC commands
- the SCM correctly sends the data locally produced
- the SCM correctly receives and internally distributes the CLOCK reference signal. In addition, it correctly executes the control instructions that it may receive along the CLOCK connection
- the SCM correctly controls and/or communicates with the devices locally connected: SPM, laser beacon, acoustic transponder, pressure (or CTD) sensor, sound velocimeter
- the SCM correctly elaborates the analog signals coming from the Laser Beacon photodiode and the acoustic transponder

Interfaces to the SCM are:

- SPM-connector: 400 VDC power from Test Bench power supply to SCM, RS485 twisted pair for SPM slow-control emulation

- JB/SPM-side: DATA/SC and CLOCK fibers (these connections will be made at the OPT_CON level)
- String-side: 6 CLOCK fibers (these connections will be made at the OPT_CON level)
- Laser beacon connector: 48 V power from SCM, RS485 twisted pair for laser beacon SC emulation, output pulse from SCM for laser drive and analog input from (simulated) photodiode to SCM
- Acoustic transponder connector: emulator for analog signal from acoustic transponder
- Pressure (or CTD) sensor connector: 48V power from SCM, RS232 serial communication with sensor emulator
- Sound velocimeter connector: 48V power from SCM, RS232 serial communication with sensor emulator
- Backplane: check that the 20 MHz clock from the Clock board is correctly distributed, interface to the internal RS485 MODBUS + others to be defined

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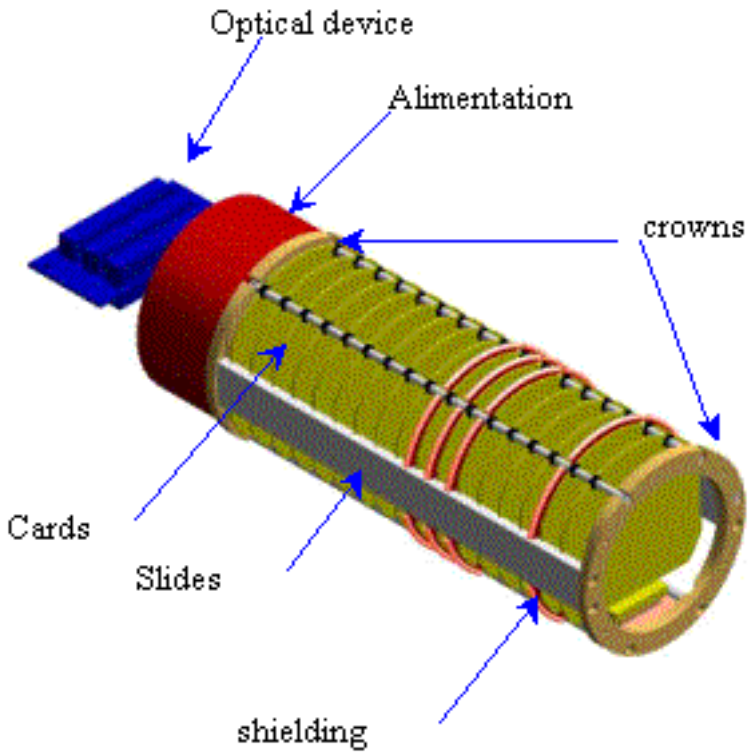
Associated Technical Notes

3 SCM 18 01/A: Proposal for a SCM Test Bench (to be released soon)

PBS2.2.001: SCM_CRATE (in SCM container)

Schematic view of the Inner rack



The design of the SCM_CRATE inner rack is:

- The SCM_CRATE inner rack houses the string control module offshore electronics.
- It consists of an axial structure that links all the cards and the backplane
- Electric and optical cables penetrate the container and are plug in cards.
- This structure looks like a cylindrical cage placed inside the SCM container and fixed in the lower bottom end cap by a crown.

Dimensions, technological features:

- Effective inner diameter: 155 mm
- Effective inner length: 550 mm
- The selected material for all part of the inner rack is aluminium 2017. Both inner and outer diameters must be chamfered

Interfaces inside SCM are:

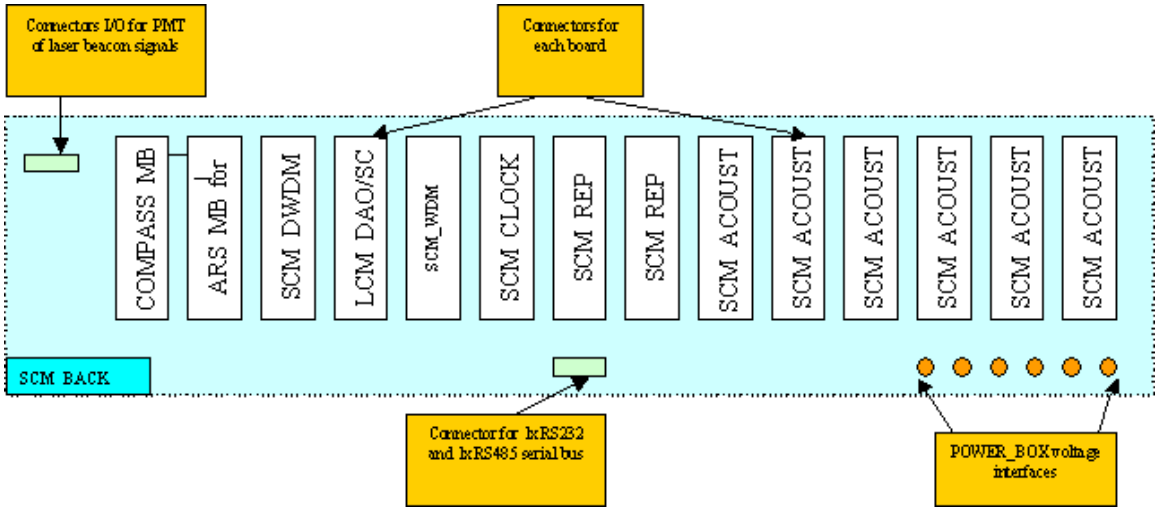
- 16 boards
- 1 electrical connection board
- 1 optical connection device
- SCM power box for voltage
- 4 shielding for OEM and thermal conduction

Associated Technical designs:

- 3 LCM 02 01:Integration LCM
- 3 LCM 02 03: shielding
- 3 LCM 02 04: crown 1
- 3 LCM 02 05: crown 2
- 3 LCM 02 06: Slides

PBS 2.2.002: SCM_BACK board (in SCM container)

Schematic diagramme of the SCM_BACK board



The main functions of the SCM_BACK board are:

- Distributes inside the SCM container all signals from or to each board inserted inside the SCM_CRATE .
- Distributes electrical power: +5V, +3.3V, +2.5V, +1.8V, +12V, +48V and common return, all these power signals come from the POWER_BOX fixed on the SCM_CRATE.
- The SCM_BACK interfaces between the optical modules signals and the ARS_MB, POWER_BOX and COMPASS_MB electronics boards.
- Each board has a fixed location in order to optimise EMC and parallel development.
- Controls the SPM container slow-control function through a second RS485 twisted pair with MODBUS protocol.

Interfaces inside the SCM are:

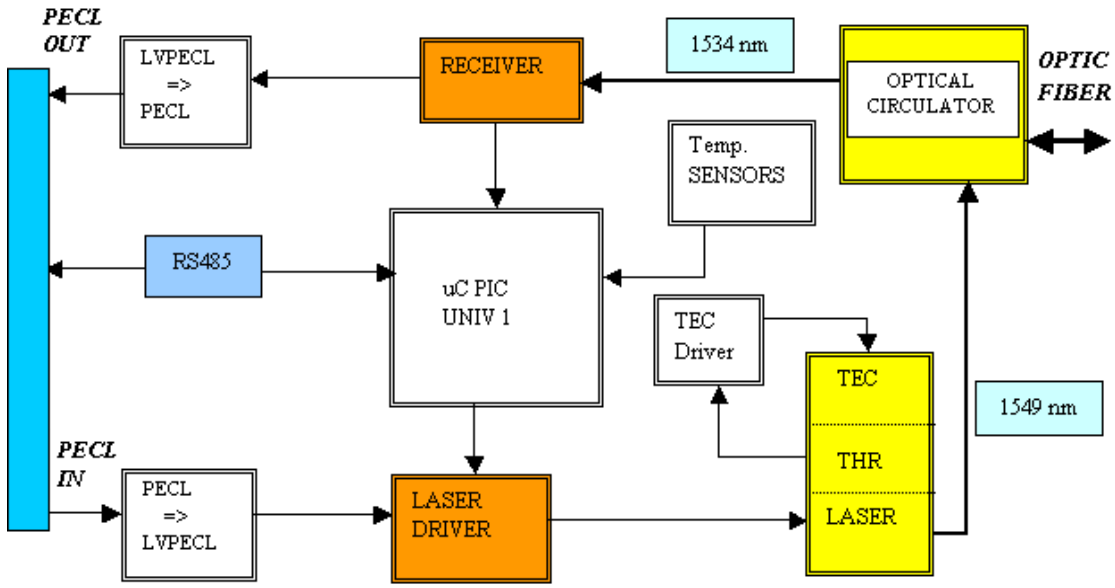
- Each board inserted in the SCM_CRATE is connected to the SCM_BACK with its rear connector (24, 48, or 96 pins).
- 1 connector interfaces with the laser beacon PMT (configuration for one line only).
- 1 connector interfaces with other containers for RS232 and second RS485 serial bus, this connector also transmits the test signal for LCM_DAQ/SC board (external test trigger signal). This connector drives also the main RS485 serial bus for all boards inserted inside SCM_CRATE in order to test slow-control without the LCM_DAQ/SC board.
- The second RS485 twisted pair controls the SPM slow control function.
- The boards inserted inside the SCM_CRATE are:
    - COMPASS_MB, ARS_MB for laser beacon, SCM_DWDM, LCM_DAQ/SC, SCM_WDM,SCM_CLOCK, SCM_REP (2 boards), SCM_ACOUST1 to 6 and

Associated Technical Notes:

3 SCM 20 01: SCM internal organisation.

PBS 2.2.003: SCM_WDM (in SCM container)

Schematic diagramme of the SCM_WDM board:



The main specifications of the SCM_WDM module are:

- Bi-directional electrical/optical module using WDM (Wavelength Division Multiplexing) concept to send the reference clock and control words from the ON_CLOCK board to all the LCM_CLOCK boards.
- Receive status words from a selected LCM_CLOCK board.
- The wavelength of the optical signals are 1535 nm from ON_WDM to SCM_WDM and 1549 nm for the opposite direction.
- The clock signal (converted in electrical PECL format) are sent to the SCM_CLOCK, SCM_REP boards in order to be regenerated and converted to optical signal for each sector.
- Slow control parameters reading for board monitoring, with UNIV1 daughter board. The main parameters are: optical signal reception, switching ON/OFF laser driver, temperature measurement.
- Temperature of the laser controlled by Thermoelectric Cooler controller (TEC) DN1220 ThermoOptics.

Interfaces to :

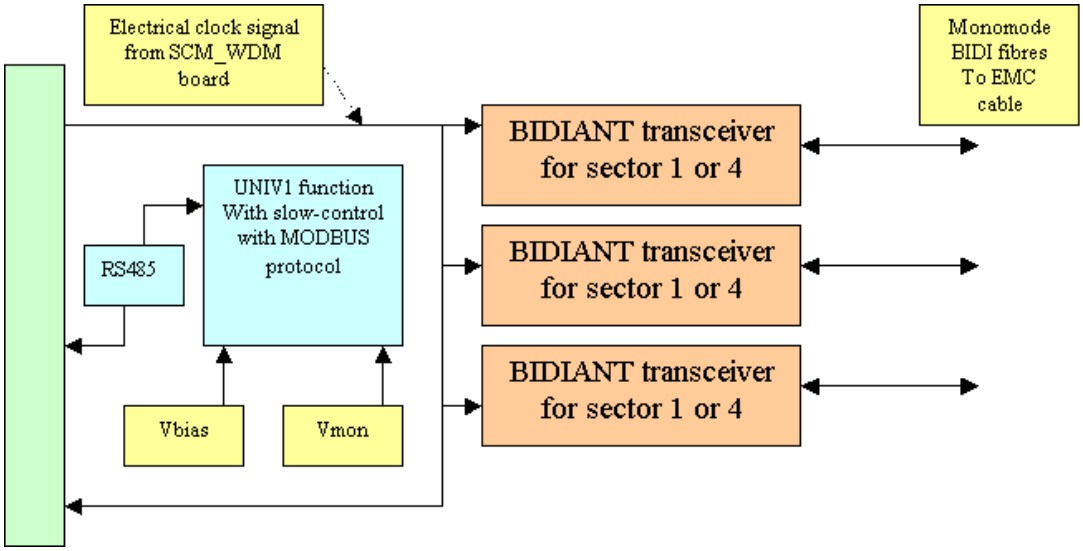
- SCM_CLOCK board through the Input/Output PECL channels (200 Mbps).
- SCM_REP board through the rear connector on SCM_BACK (200 Mbps)

Technical Notes associated on WEB page:

- 3 SCM 02 01/B: SCM internal organisation
- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 03 02 : Clock Distribution ON_SHORE for ANTARES (Proposal)
- 3 LCM 08 04: BIDIANT user's manual

PBS2.2.004: SCM_REP board (in SCM container)

Schematic of the SCM_REP board


Electrical clock signal from SCM_WDM board
Monomode BIDI fibres To EMC cable
BIDIANT transceiver for sector 1 or 4
BIDIANT transceiver for sector 1 or 4
BIDIANT transceiver for sector 1 or 4
UNIV1 function With slow-control with MODBUS protocol
RS485
Vbias
Vmon

The main specifications of the SCM_REP board are:

- Electrical to optical conversion between SCM_WDM board and each sector for clock distribution function.
- Electrical to optical conversion through the BIDIANT daughter boards plugged on SCM_REP board.
- The UNIV1 function allows monitoring of the Vbias and Vmonitor voltage of each BIDIANT daugther boards and one temperature sensor.
- Inside each SCM container, we have 2 SCM_REP boards in order to drive clock signals for the 6 sectors of a line.

Interfaces inside SCM are:

- Clock electrical signal goes from SCM_WDM to SCM_CLOCK and SCM_REP (first) and SCM_REP (second) in serial topology via a PECL twisted pair.
- DAQ board for clock signal, reset/enable and slow_control RS485 bus by twisted pairs on backplane
- SCM_WDM board with twisted pairs PECL (clock signal) on backplane SCM_BACK.
- POWER_BOX for voltage (+5V and +3.3V) by backplane

Associated Technical Notes:

3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)

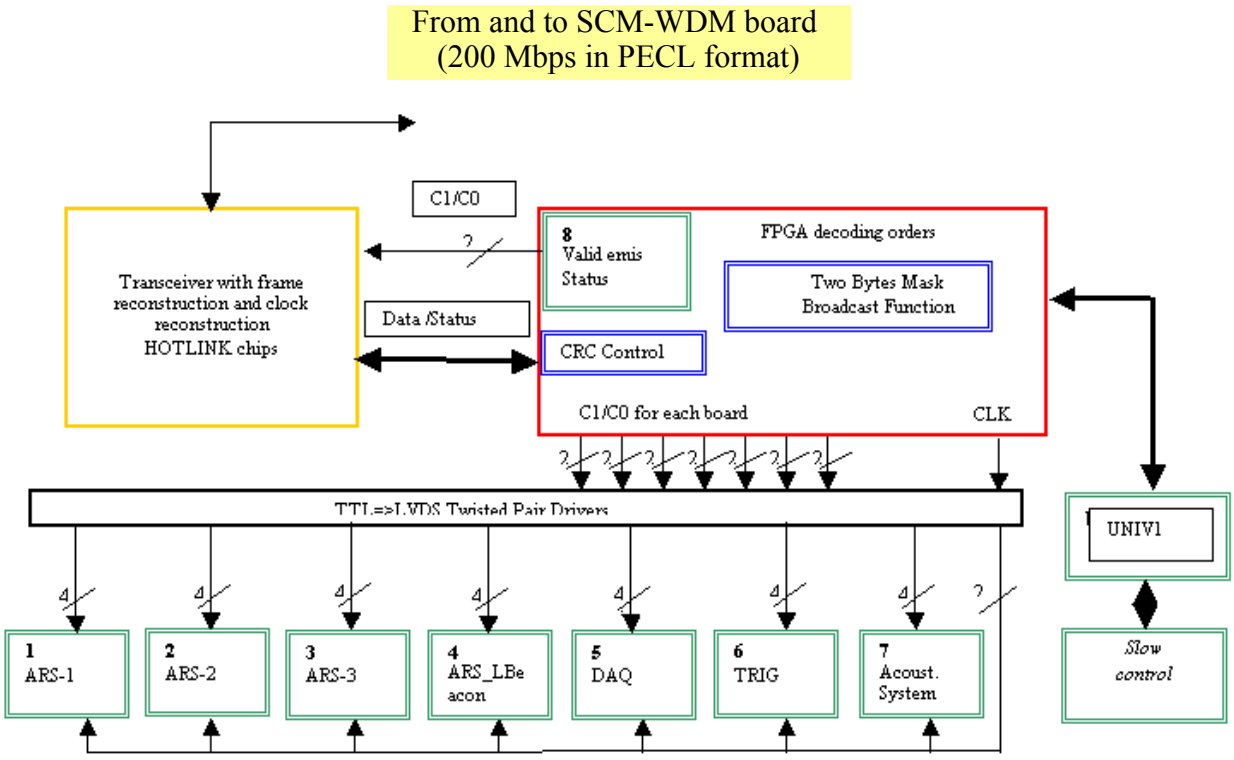
3 LCM 03 02: Clock Board interfaces description

3 LCM 18 02: Clock distribution prototypes tests

3 SCM02 01: SCM internal organisation

PBS2.2.005: SCM_CLOCK board (in SCM container)

Schematic view of the Clock board



Specifications:

- Distribution inside SCM container of the reference clock (20 MHz) from shore to all boards which use this signal for physics time stamp for example (ARS boards).
- Generation of synchronous signals for ARS (Enable/Reset), DAQ (Enable/Reset), Acoustic positioning system (low rate and high reset), Trigger (Enable/window pulse)
- Return path possibility in order to read status byte from specific LCM to shore station
- Slow control parameters reading for board monitoring, with UNIV1 daughter board. The main parameters are: optical signal detection, temperature measurement, laser bias current and modulation, byte status, filter addressing mask configuration, etc..

Interfaces inside SCM are:

- DAQ/SC board for clock signal, reset/enable and slow_control RS485 bus by twisted pairs on backplane
- SCM_WDM board with twisted pairs PECL on backplane SCM_BACK.
- Acoustic board (SCM_RxTx boards) for clock signal, and resets by twisted pairs on backplane.
- ARS boards for clock signal and reset by twisted pairs on backplane.

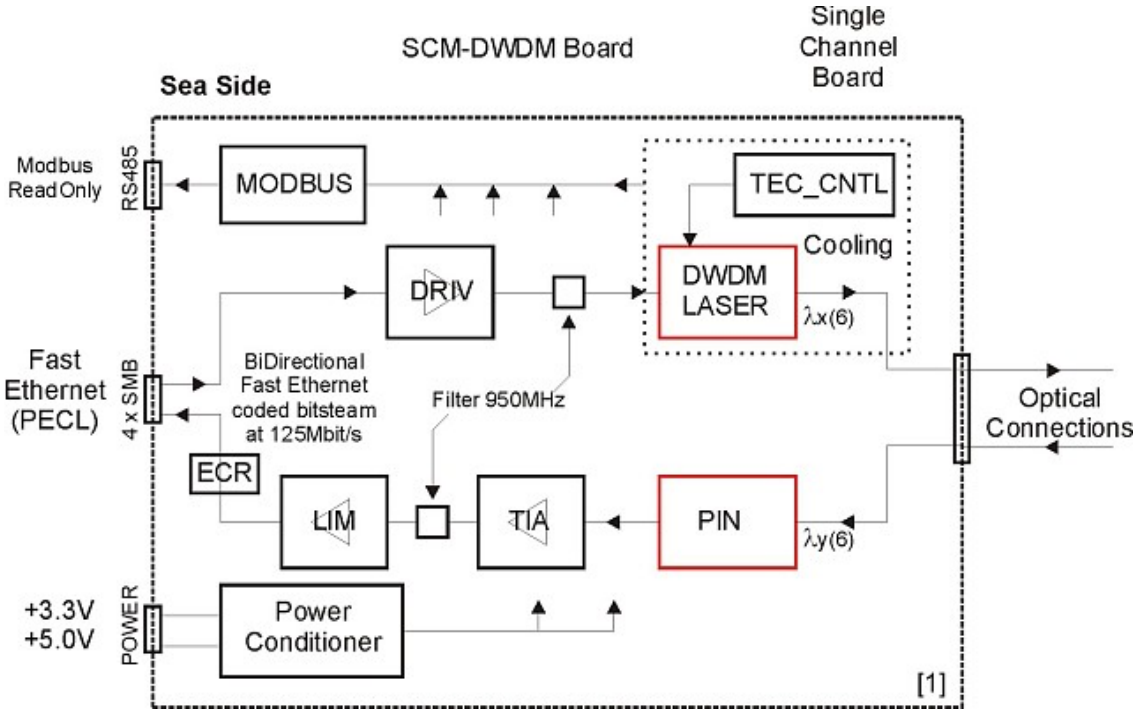
- ARS laser beacon for clock signal and reset by twisted pair on backplane.
- POWER_BOX for voltage (+5 V and +3.3 V) by backplane

Technical Notes:

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 03 02: Clock Board interfaces description
- 3 LCM 18 02: Clock distribution prototypes tests
- 3 SCM02 01: SCM internal organisation

PBS 2.2.006: SCM-DWDM Board (in SCM container)

Schematic diagramme of the SCM-DWDM Board:



The SCM-DWDM Board converts the Fast Ethernet signals from the DAC/SC Board into the optical signals of a Dense Wavelength Division Multiplexing (DWDM) system and vise versa. Important parts on this board are the DWDM Laser and the Pin-Diode Receiver. The DWDM Laser is a Distributed Feedback type with very narrow spectral width, operating in the 1550nm range at 1.25 Gb/s. The system is based on the ITU grid standards for DWDM applications with 400 GHz channel spacing.The specific optical ITU-channel wavelength λ_x is obtained by very accurate temperature control with a Thermo-Electric Cooler (TEC). Temperature stabilisation of < 0.1°C is needed for 0.1nm wavelength locking. The Pin-Diode Receiver with Trans Impedance Amplifier (TIA) and Limiting Amplifier (LIM) converts the optical signal λ_y back to an electrical signal.

The main specifications of SCM-DWDM Board are:

- Electro-Optical conversion and vice versa of Fast Ethernet 100BASE-TX signals.
- DWDM Laser temperature control to < 0.1°C.
- Slow control parameters Read-Only for board monitoring, with UNIV1 daughter board. The main parameters are: optical signal detection, laser temperature measurement, laser wavelength lock, laser bias current and laser modulation current.

Interfaces inside SCM are:

- DAQ/SC Board for Slow-Control, RS485 bus by twisted pairs on SCM backplane.

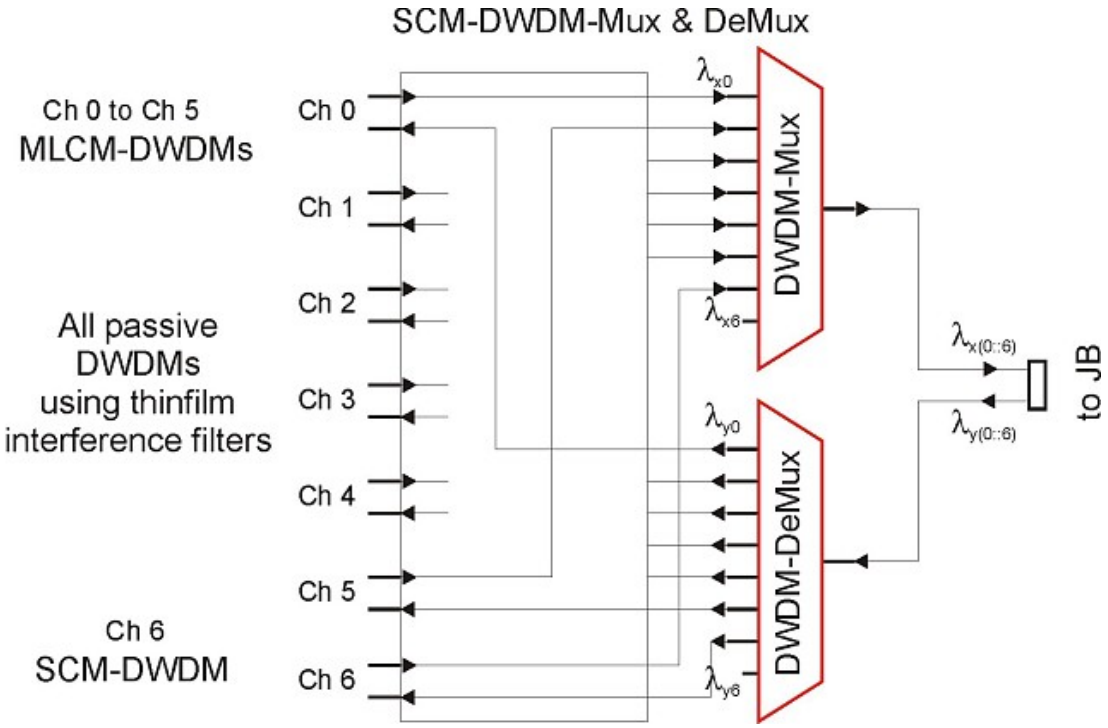
- DAQ/SC Board Fast Ethernet signals via coaxial SMB connectors.
- Optical I/O to the SCM-DWDM-MUX & DEMUX
- Backplane for Supply Voltages; 3.3V and 5.0V.

Associated Technical Notes:

- http://www.nikhef.nl/~n05/antares/ETR_Notes/ETR2000-07s.pdf
- http://www.nikhef.nl/~n05/antares/ETR_Notes/ETR2000-08s.pdf

PBS 2.2.014: SCM-DWDM-MUX & DEMUX (in SCM container)

SCM-DWDM-MUX & DEMUX schematic:



The SCM-DWDM-MUX & DEMUX is a passive optical circuit inside the SCM container. Optical signals to and from the MLCMs are split/combined with Dense Wavelength Division Multiplexers and Demultiplexers. The optical signals; $\lambda_{x(0:6)}$, 6 wavelengths from the MLCMs for DAQ and 1 for SCM-SC, are multiplexed with a DWDM Multiplexer into a single mono mode fiber. The optical signals from the JB (Shore Station), $\lambda_{y(0:6)}$ are demultiplexed with a DWDM-Demultiplexer into 7 output fibers. Two sets of 6 wavelengths are used for DAQ -Gigabit Ethernet- and a 7th set is used for SCM-SC (Fast -100Mb- Ethernet).

The DWDM Multiplexer and DWDM Demultiplexer use thin film interference filters, the optical path is epoxy free. The ITU wavelength grid used for these DWDMs is 400 GHz (~3.2 nm). The DWDM channels have a minimum bandwidth of 0.8 nm.

The main functions of SCM-DWDM-MUX & DEMUX are:

- Multiplexing and demultiplexing of optical signals. Optical signals are ITU defined channel wavelengths in the 1550 nm band on a 400 GHz grid. All optical parts are passive.

Interfaces inside SCM are:

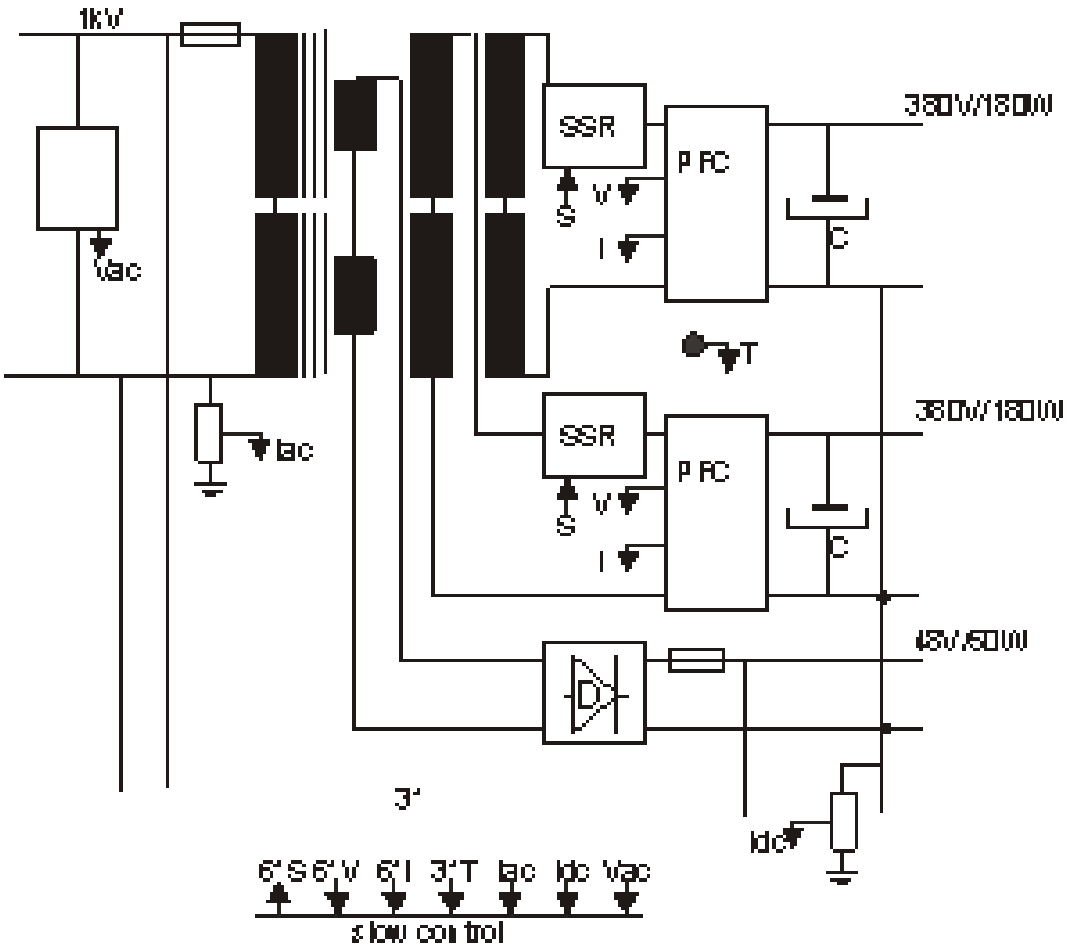
- Optical I/O to E/O-O/E Board for Slow-Control of the SCM
- Optical I/O from the MLCMs and to the JB.

Associated Technical Notes:

- http://www.nikhef.nl/~n05/antares/ETR_Notes/ETR2000-07s.pdf
- http://www.nikhef.nl/~n05/antares/ETR_Notes/ETR2000-08s.pdf

PBS 2.3 : The String Power Module (SPM)

Schematic view of the SPM



The String Power Module (SPM) is fed by the 1000 Vac of the Junction Box. It converts the 1000 Vac to 400 Vdc for use in the LCMs of a string. It also provides 48 Vdc for the control systems of the SPM and SCM.

The SPM consists of three pairs of ring core transformers, each pair feeds two sectors and each has a fuse to prevent shorting of the 1000 V by a single transformer. Each output has a Solid State Relay (SSR) which isolates a sector in the case of failure inside a LCM. A Power Factor Corrector (PFC) circuit provides an almost resistive load to the transformer, giving high efficiency rectification and low noise.

All output currents, voltages and the supply temperatures are monitored by the Slow Control UNIV board. All outputs can be switched on/off by remote control. Over-temperature and over-current situations are handled locally.

The thermal cooling of the SPM is understudy, the preferred solution is that adopted for the LCM container, in which copper fingers connect to the walls of the SPM container. Further details can be found in the internal note on SPM.

The components used satisfy military specifications, the expected MTBF is of the order of 50 years.

Specifications:

Input

Voltage to activate the local slow control	680-1000 V
Voltage to deliver 6* output	720-1000 V
frequency range	48-55 Hz
power factor	>0.97
Cos phi	>0.95
Nominal power	1300 W

Output: 6* 380 Vdc

voltage variations	<5%
ripple	<10%tt
noise	<1%tt
nominal power	180 Watts
maximum power	200 Watts
overload protection	fuse

Output: 1*48 Vdc

voltage variations	<5%
ripple	<10%tt
noise	<1%tt
nominal power	50 Watts
maximum power	60 Watts
overload protection	fuse

Monitoring

1* ac input voltage
6*dc output voltages
6*dc output currents
1*ac leakage current to container 0-10mA
1*dc-leakage current to container 0-10mA

Interfaces

- JB via an Interconnecting Link cable
- SCM

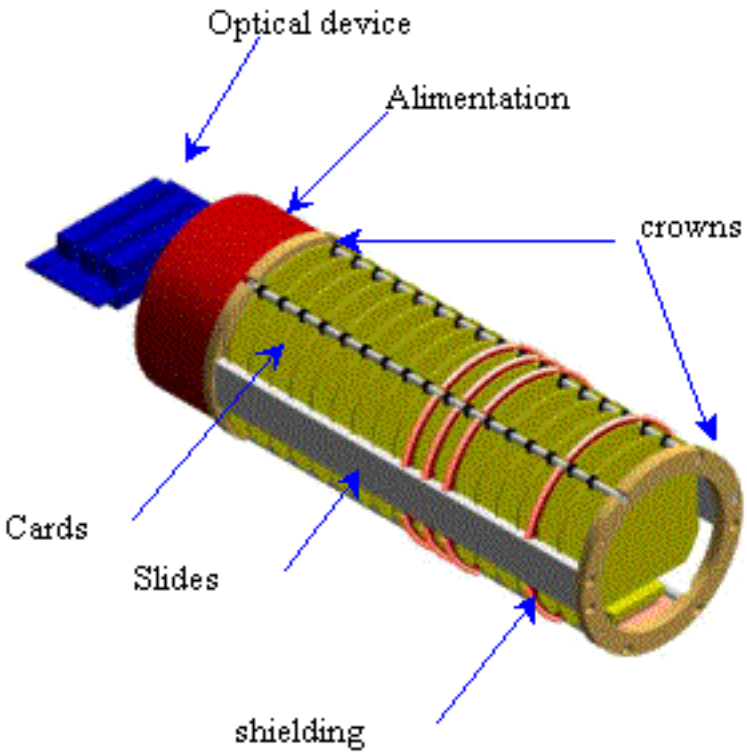
Objects in SPM	Description	PBS number
SPM_CONTAINER	contains all the items below	1.2.007
SPM_CRATE	support of boards and backplane	2.3.001
SPM_BACK1	distributes signals between boards in SPM_CRATE	2.3.002
SPM_CONNECT1	connections inside SPM	2.3.003
SPM_CONNECT2	connections inside SPM	2.3.004
SPM_CONT1	controls power distribution	2.3.005
SPM_CONT2	controls power distribution	2.3.006
SPM_CONT3	controls power distribution	2.3.007
SPM_CONT4	controls power distribution	2.3.008
SPM_LV	Produces low voltage	2.3.009
SPM_TRANS1	transformer for HV AC	2.3.010
SPM_FILT1	electrical filter for power conversion	2.3.011
SPM_REGUL	Voltage regulator	2.3.012
SPM_DC/DC	DC/DC conversion	2.3.013
SPM_FILT2	Electrical filter on output	2.3.014
SPM_HEAT1	Heat dissipator	2.3.015
UNIV1	Daughter board plugged on other board for slow control MODBUS interface	2.1.013

List of References

- Power section in Chapter 7
- SPM technical note, to be released soon.

PBS 2.3.001: SPM_CRATE (in SPM container)

Scheme of the Inner rack



The design of the

SPM_CRATE is:

- The SPM_CRATE inner rack houses the String Power Module electronics.
- It consists of an axial structure that links all the cards and the backplane
- Electric and optical cables penetrate the container and connect to the relevant cards.
- This structure looks like a cylindrical cage placed inside the SPM container and is fixed at the lower lid cap by a crown.

Dimensions, technological features:

- Effective inner diameter: 155 mm
- Effective inner length: 550 mm
- The selected material for all part of the inner rack is aluminium 2017. Both inner and outer diameters must be chamfered

Interfaces inside SPM are:

- 16 boards
- 1 electrical connection board
- 1 optical connection device

- LCM power box for voltage
- 4 shielding boards for OEM and thermal cooling

Associated Technical drawings at:
http://antares.in2p3.fr/internal/deci-km2/tableaux/LCM.htm

- 3 LCM 02 01:Integration LCM
- 3 LCM 02 03: shielding
- 3 LCM 02 04: crown 1
- 3 LCM 02 05: crown 2
- 3 LCM 02 06: Slides

15/02/2001 M.Jaquet/P.Lagier

The Junction Box list of objects

The Junction Box (JB) is the heart of the ANTARES detector. It receives Power from the onshore Power Hut via the Main Electro-Optical Cable (MEOC) and distributes it to the strings via the Interconnecting Links (IL). Data, Clock, Trigger and Control signals also transit via the JB through the same cables.

Components are separated into mechanics, electronics and power aspects and each of these aspects is described separately in the corresponding chapter.

Since it is is the first detector system we build, to be installed in the sea, it has the first PBS number. The associated PBS numbering has been fixed by the collaboration organisational structure (starting with 1 for mechanics, 2 for electronics and 6 for power). A list of the components can be found below.

- **PBS 1. 1 Junction Box: mechanics part**

PBS1.1.1	JB Frame	
PBS1.1.2	JB_Container	
PBS1.1.2.001	JB Vessel	2 Ti hemispheres and 1 cylind. spacer
PBS1.1.2.002	JB Diaphragm	separates the transformer to the electronic volumes
PBS1.1.2.003	Feed-throughs	transmit power and diagnostic (7)
PBS1.1.2.004	PRE-JB	holds penetrator for connection to EO cable
PBS1.1.2.005	JB O-ring	
PBS1.1.2.006	Balancing device	
PBS1.1.3	Acoustic Beacon support	
PBS8.1.5	LBL Acoustic Beacon	gives the position of the frame

- **PBS 2.4 Junction Box clock distribution and trigger construction**

PBS2.4.001	JB_ELECBOX	contains electronics boards
PBS2.4.002	JB_SPLIT1	passive splitters for clock distribution
PBS2.4.003	JB_TRIG1	RoR signal construction
PBS2.1.013	UNIV1	Daughter board plugged on other board for slow control MODBUS interface

- **PBS6.4: Junction Box (Power part)**

PBS6.4.1	Penetrators and bulkhead receptacles

PBS6.4.2	Power components
PBS6.4.3	Power Remote diagnostic
PBS6.4.4	Very Low Voltage Power Supply
PBS6.4.5	Cabling and Connections
PBS6.4.6	Sensors
PBS6.4.7	Remote Control

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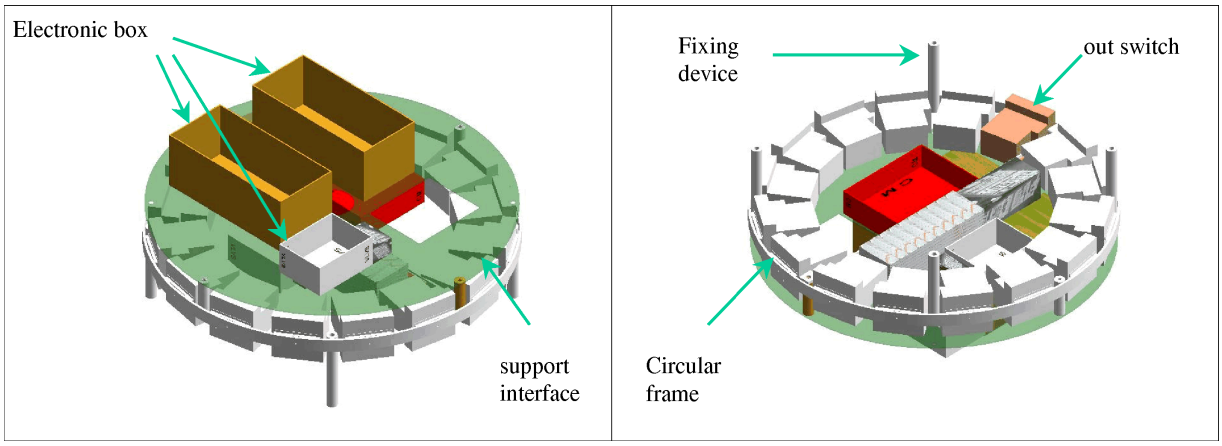
links to TDR

- Junction Box Mechanical Description
- Electronics Power Distribution
- Electrical Power system

PBS2.4.001: JB ELECBOX

Schematic views of the JB ELECBOX



Requirements

- The main mechanical function is to support all the electronics box.
- An assembly has been performed
- All presently defined parts fit in
- Connection and accessibility tests : to be done
- Assembly on JB container tests : will be done in CPPM

Listing components in electronics box

- 16 out switch 105x116x130
- 7 out ctl 102x33x95
- 1 out sensor60x60x60
- 1 clock + ROR 320x150x126
- 1 control module 320x150x126
- 1 low volt 256x131x100
- 1 EOC terminal110x170x150
- 1 electrode Terminal110x170x50
- 1 current meas 250x200x65
- 1 relay 200x135x63
- 2 relays 130x90x60

Dimensions, technological features:

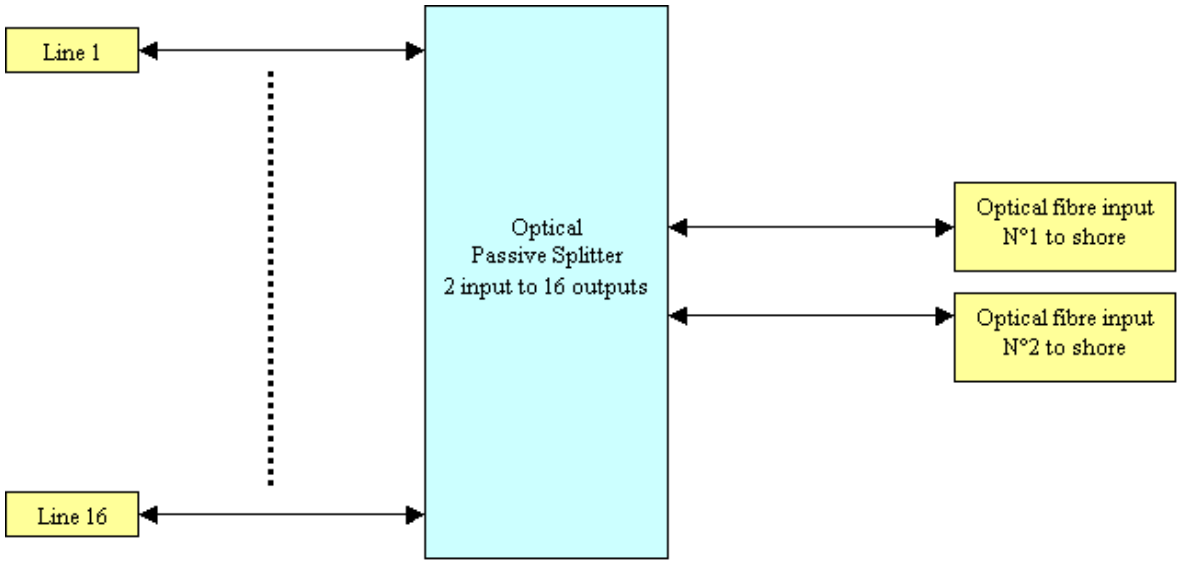
- Support interface diameter: 800 mm
- Total height: 373 mm

Technical design

3 BJO-04-01 A	Ensemble interne JB

PBS 2.4.002: JB-SPLIT board (in Junction Box container)

Schematic diagramme of the JB-SPLIT board:



The main specifications of the JB_SPLIT board are:

- Distribute to all lines of the detector optical clock signal with a division (splitting function) from 2 fibres to 16 outputs fibres.
- Two optical fibres come from shore in order to have a redundancy capability for better reliability.
- The reference of this optical component from E-TEK company is TWSCBE00PH215, we can find more details about this component in E-TEK company web page: www.e-tek.com.

Interfaces inside JB are:

- Inputs and outputs optical fibres are connected to optical fibres which come from MEOC and each JB to the Interconnecting links by an optical connector from Deutsch company OPTOCLIP II standard.
- No electrical power needs, passive component.

Picture of this component, inserted in crate for tests and measurement

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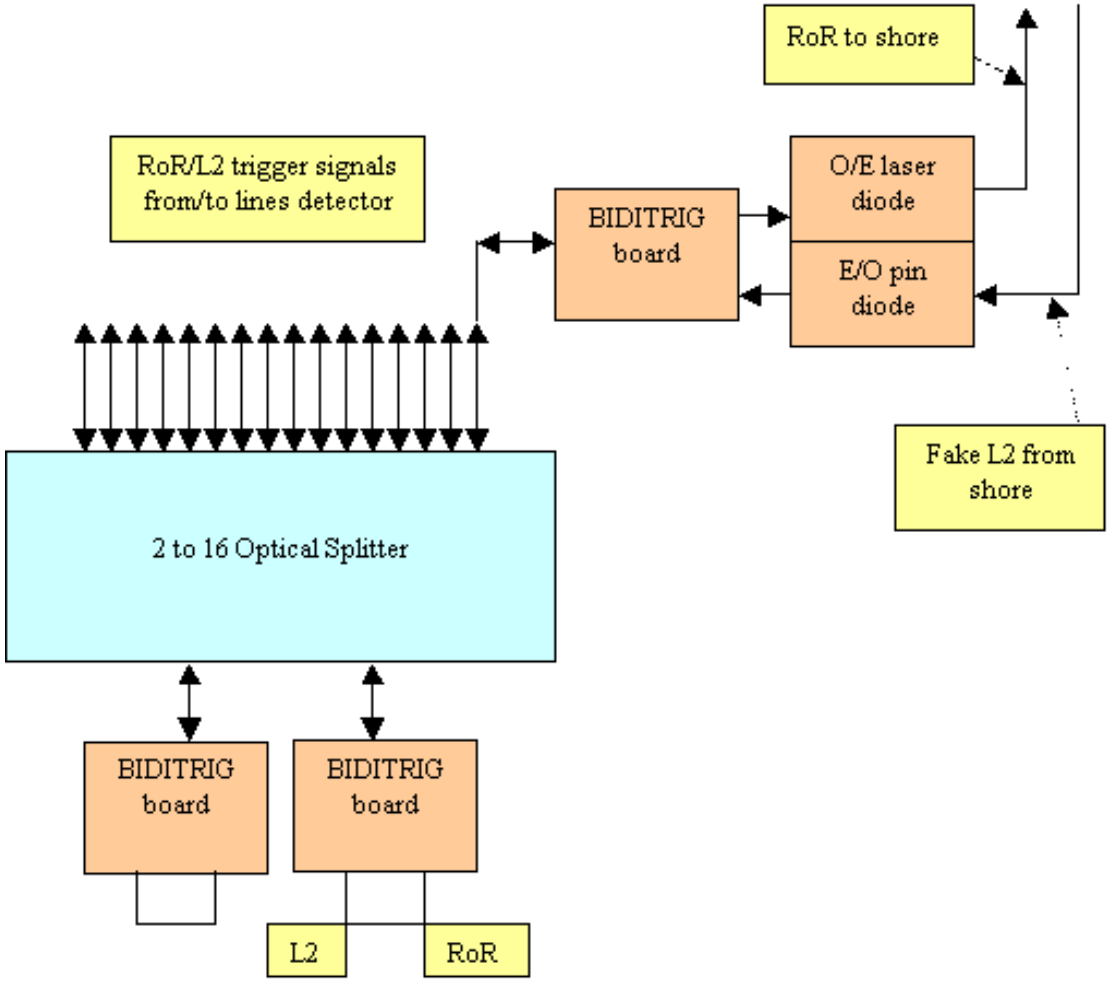
Technical Notes

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 18 02: Clock distribution prototypes tests

PBS2.4.003: JB-TRIG board (JB container)

Schematic of the JB-TRIG transceiver board:



The main specifications of the JB-TRIG transceiver board are:

- Concentrate all L2 signals from each string of the detector and return the RoR signal to all lines.
- This OR function is built with an optical splitter with 16 channels inputs and 2 channels outputs (2 for redundancy).
- The optical OR signal (between all L2 signals) is converted to an electrical signal which is returned after an O/E/O conversion in a BIDITRIG board. A second BIDITRIG board can be used if the first fails.
- A spare channel optical channel is sent to shore in order to monitor the RoR signals of the detector. Two fibres are reserved inside the MEOC for this function.
- A pair of optical fibres are reserved to allowing sending of a 'fake' L2 signal from shore.

Interfaces inside LCM and JB are:

- The BIDITRIG daughter board has standard TTL input and output with +5V power voltage.The BIDITRIG incorporates standard BIDI component with pigtail and standard OPTOCLIP II connector on optical fibre.
- The reference of this optical splitter 2 to 16 from E-TEK company is TWSCBE00PH215, more details about this component can be found in E-TEK company web page: www.e-tek.com
- Power needs for this JB-TRIG board is produced internally by a DC/DC converter with standard 24 Volts input produced by the power box in the Junction Box.

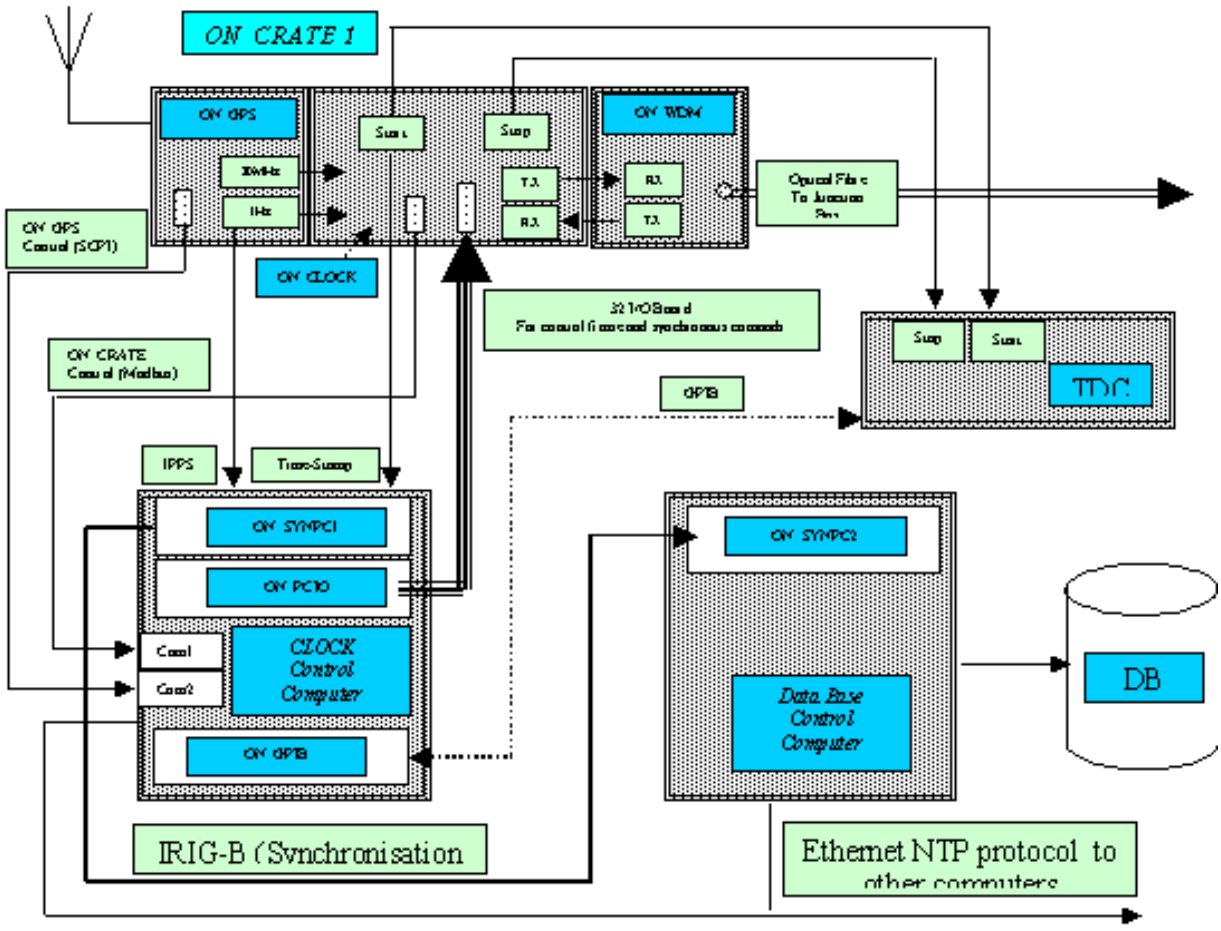
PBS2.5: On shore Clock objects

The clock is produced on shore and sent to all the storeys. The function is described in the relevant Electronics section about the clock distribution.

Object in Onshore CLOCK container	Description	PBS number
ON_CRATE1	Electronics crate	2.5.001
ON-GPS	GPS receiver producing reference signal for clock distribution	2.5.002
ON_CLOCK	Coding /decoding orders for clock distribution	2.5.003
ON_WDM	Optical transceiver for clock distribution	2.5.004
ON_SYNCPC1	PC board	2.5.005
ON_PCIO	digital interface for ON_CLOCK board	2.5.006

PBS 2.5.001: ON_CRATE1 (ON SHORE)

ON_SHORE schematic diagramme



The ON_CRATE1 contains several boards in Europe format (100X160) :

- ON_GPS module with GPS (Global Positioning System) *REF HP 58540A*, including frequency doubler *REF TLC2932 EVM.*
- ON_CLOCK module for interfacing the Clock Control Computer to the ON_WDM module.
- ON_WDM (Wavelength Division Multiplexing) optical module connected to the Junction box JB_SPLIT1.

To Clock Control Computer:

- ON_PCIO is a fast interface PC board for sending address commands to ON_CLOCK module
- ON_SYNCPC connected to *1PPS* and *Time-Stamp* from ON_CLOCK outputs (Synchronize function).

- **Com1** using a Slow Control MODBUS protocol for ON_CRATE1 Monitoring function.
- **Com2** using *SCPI* protocol for ON_GPS monitoring function.

To TDC (Time to digital convert):

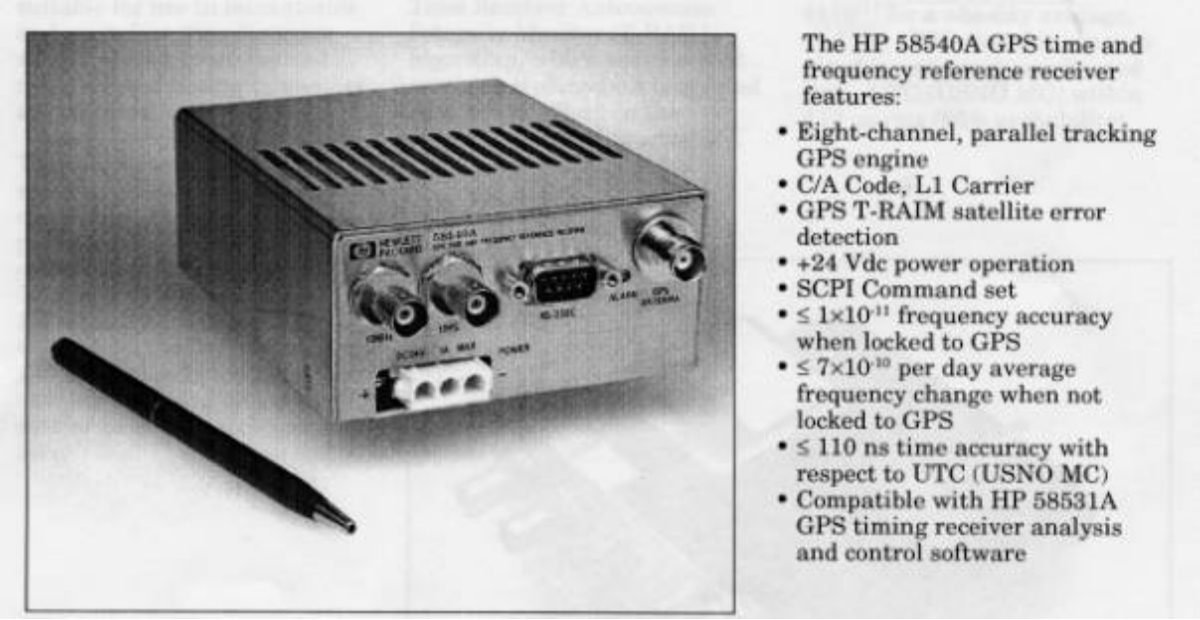
- Start/stop: Outputs TTL pulse for propagation time measurement between the onshore station and all offshore modules.

Technical Notes:

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 03 02 : Clock Distribution ON_SHORE for ANTARES (Proposal)

PBS 2.5.002: ON_GPS (ON SHORE)

ON_GPS (Global Positioning System)


The HP 58540A GPS time and frequency reference receiver features:
• Eight-channel, parallel tracking GPS engine
• C/A Code, L1 Carrier
• GPS T-RAIM satellite error detection
• +24 Vdc power operation
• SCPI Command set
• ≤ 1×10⁻¹¹ frequency accuracy when locked to GPS
• ≤ 7×10⁻¹⁰ per day average frequency change when not locked to GPS
• ≤ 110 ns time accuracy with respect to UTC (USNO MC)
• Compatible with HP 58531A GPS timing receiver analysis and control software

The main specifications of the ON_GPS module are:

- Provide a high accuracy clock 20 MHz (+/- 50ps jitter) to the offshore electronic boards.
- Provide the absolute date and time in coincidence to the UTC (Universal Coordinated Time).

Interfaces:

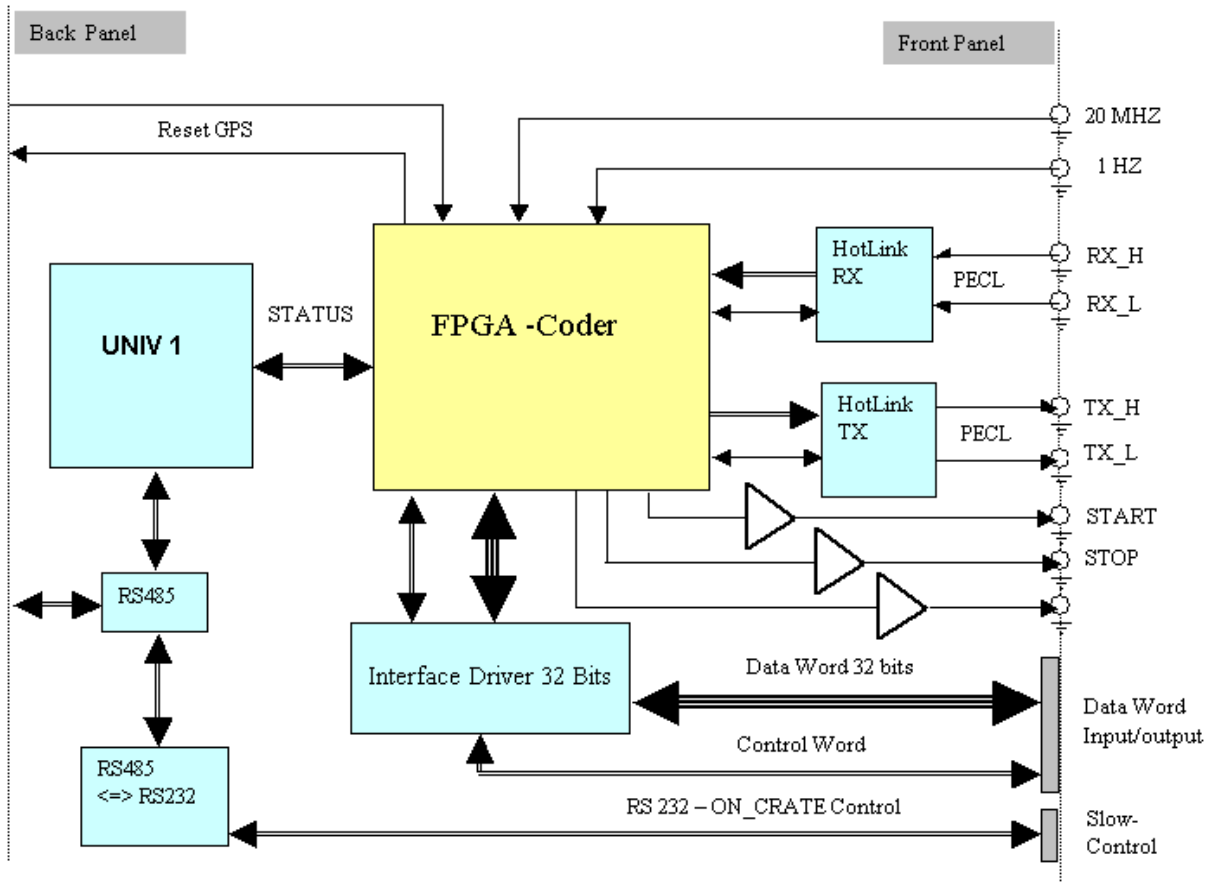
- The 20 MHz square signal is provided by a frequency doubler (TLC2932 EVM) from the 10 MHz GPS clock. This reference clock is connected to the input clock ON_CLOCK board.
- The 1 PPS output provides to the PC_CLOCK a synchronized signal in coincidence to the UTC.
- A RS232 interface allows keeping date, time and GPS monitoring by using SCPI protocol.

List of References

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 03 02 : Clock Distribution ON_SHORE for ANTARES (Proposal)

PBS 2.5.003: ON_CLOCK (onshore)

Schematic view of ON_CLOCK board



The main specifications of the ON_CLOCK module are:

- Shape and send control words from PC_CLOCK to the WDM optical module at 200 Mbps speed.
- In the receive mode, shape the status frame from the offshore modules.
- Provide START and STOP signals corresponding to the sending and receiving frames for the propagation time measurement.
- Provide a control signal for the time-stamp function.

Interfaces to :

- ON_WDM connected by twisted pairs in PECL logic for the send mode and receive mode.
- ON_PCIO PC board connected it by large cable (32 bits) for the sending control words.
- TDC (Time to Digital Convert) from *start* and *stop* output signal .

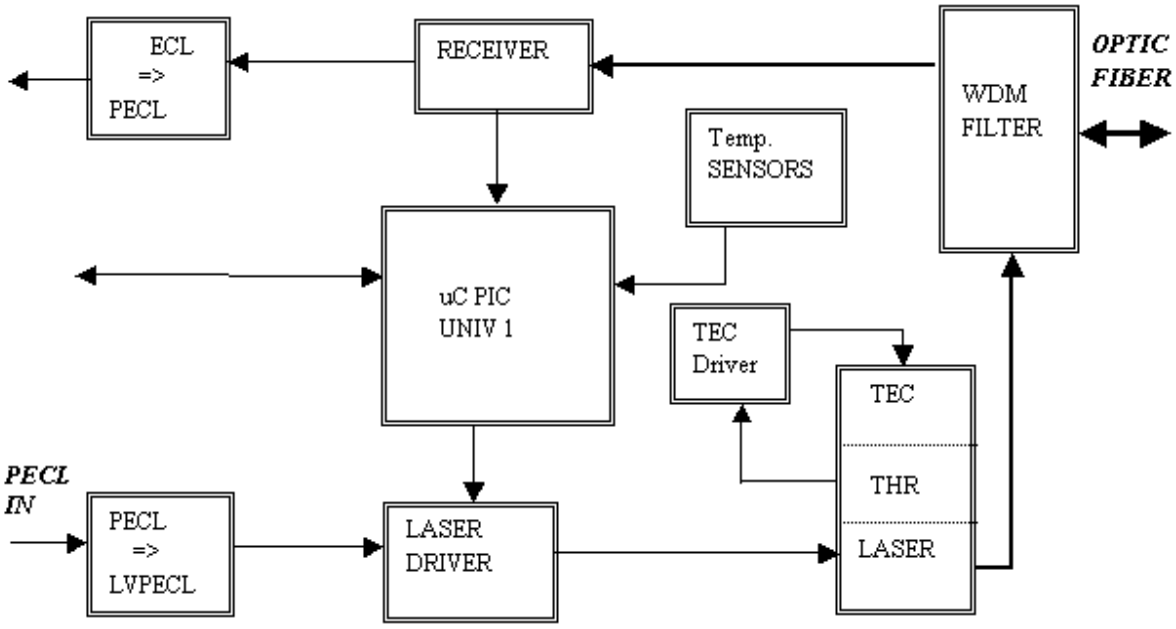
- ON_SYNCPC1 board to provide a heartbeat rate needed for the PC onshore synchronization.
- Slow Control for board monitoring.

List of References

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 03 02 : Clock Distribution ON_SHORE for ANTARES (Proposal)

PBS 2.5.004: ON_WDM (onshore)

Schematic diagramme of the ON_WDM board:



The main specifications of the ON_WDM module are:

- Bi-directional electrical/optical module using WDM (Wavelength Division Multiplexing) concept to send the reference clock and control words from ON_CLOCK to all LCM_CLOCK boards. Receive status words from selected LCM_CLOCK board.
- The wavelength of the optical signals are 1535 nm from ON_WDM to SCM_WDM1 and 1549 nm for the opposite direction.
- Slow control parameters reading for board monitoring, with UNIV1 daughter board. The main parameters are: Optical signal reception, Switching ON/OFF laser driver, Temperature measurement.
- The temperature of the laser is controlled byThermoelectric Cooler controller (TEC) *DN1220 ThermoOptics.*

Interfaces to :

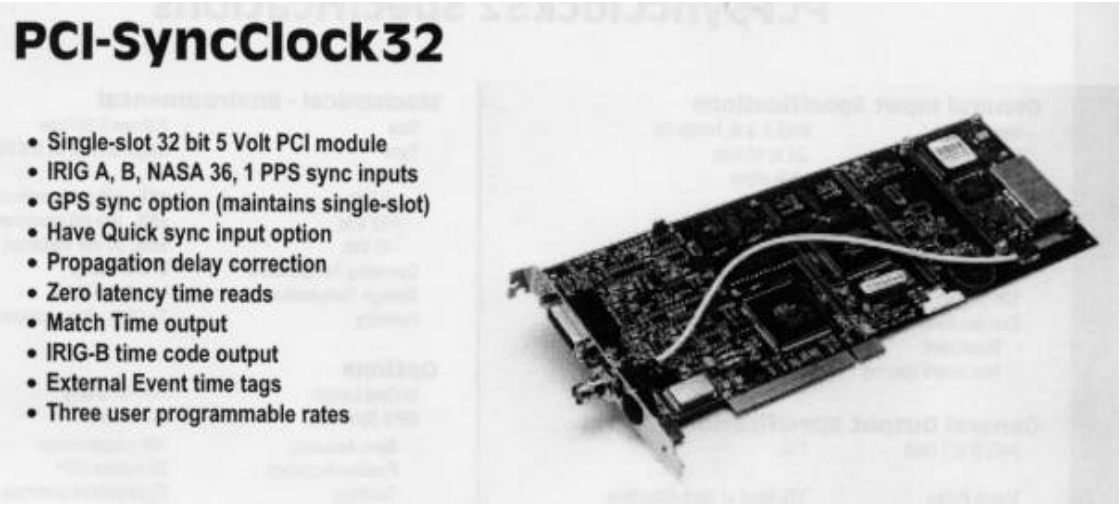
- ON_CLOCK board through the Input/Output PECL channels (200 Mbits/s).
- SCM_WDM1 boards through the shore cable Optical fibre (50 Km).
- ON_CRATE1 for the Slow control functions by RS485.

List of References

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 03 02 : Clock Distribution ON_SHORE for ANTARES (Proposal)

PBS 2.5.005: ON_SYNCPC1 (ON SHORE / PC- CLOCK)

PCI-SYNCCLOCK32 BRANDYWINE board:


PCI-SyncClock32
• Single-slot 32 bit 5 Volt PCI module
• IRIG A, B, NASA 36, 1 PPS sync inputs
• GPS sync option (maintains single-slot)
• Have Quick sync input option
• Propagation delay correction
• Zero latency time reads
• Match Time output
• IRIG-B time code output
• External Event time tags
• Three user programmable rates

The main specifications of the ON_SYNCPC1 module are:

- Provide absolute Date and Time in relationship with the UTC signal from the GPS.
- Provide Time-stamp of the control word sending with 100ns precision time.
- Provide IRIG B protocol generator allowing absolute Date and Time sending to other computer.

Interfaces to:

- GPS/UTC (Universal coordinated Time) output for synchronous time function
- ON_CLOCK board from Time-stamp output to the PC-SYNC Event time tags input.
- IRIG-B generator output to reception of IRIG-B PC Board with another computer.

List of References

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- 3 LCM 03 02 : Clock Distribution ON_SHORE for ANTARES (Proposal)
- **http://www.brandywinecomm.com**

PBS2.5.006: ON_PCIO (onshore PC- CLOCK)

PCIO-DIO-32HS National Instruments board:

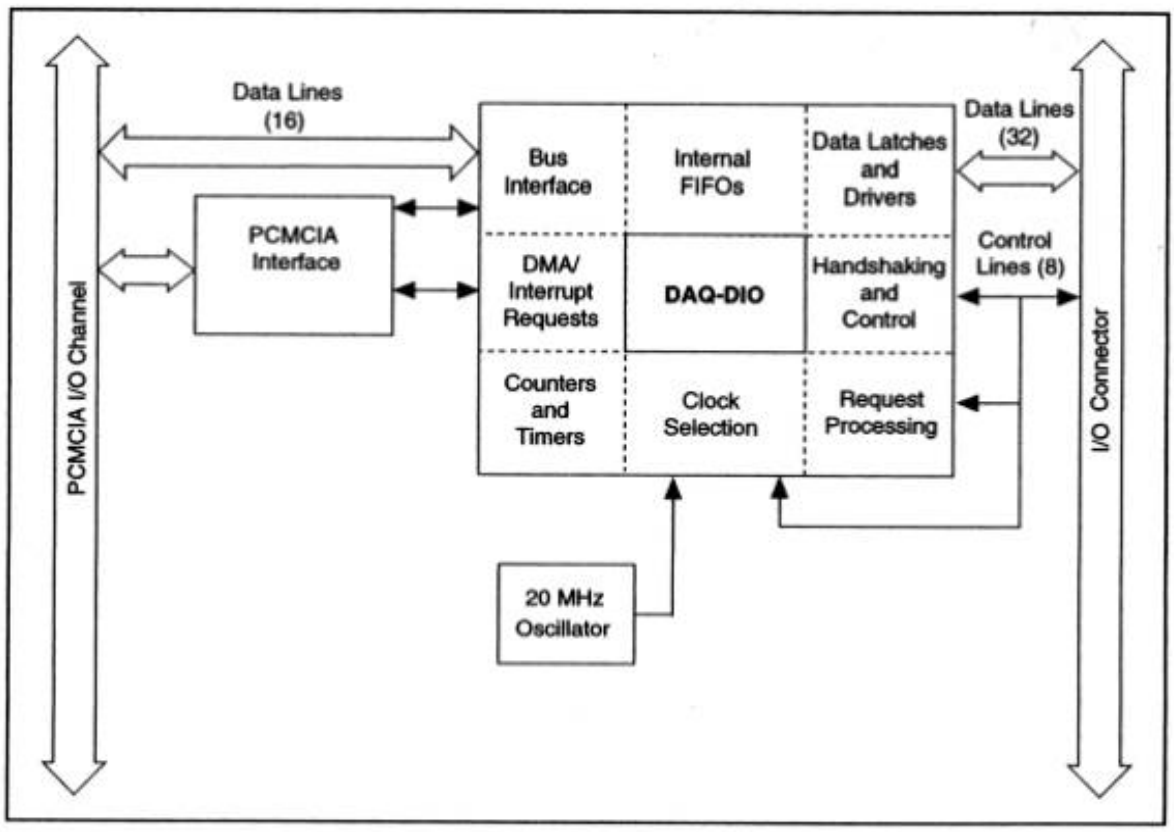


Figure 3-3. DAQCard-6533 Block Diagram

The main specifications of the ON_PCIO board are:

- Provide a high-speed data transfer for the control word sending from users to the OFF_SHORE modules (Word / 1us, Typical).
- Located in the PC_CLOCK control
- Protocol OUTPUT/16 bits – INPUT/8 bits with Handshaking mode and 8 control lines.
- Driver Software NI-DAQ for LABVIEW / Labwindows-CVI.

Interfaces to :

- Connected to ON_CLOCK module by large cable (Data lines (32) – Control lines (8)).
- Remote computers (through PC_CLOCK) by Ethernet to provide remote control word sending .

List of References

- 3 LCM 03 01: Numerical clock distribution for ANTARES (Proposal)
- **http://www.ni.com**